A STUDY ON OPTIMAL LAYOUT OF CMOS FUNCTIONAL ARRAYS

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ABSTRACT

The objective of this project is to build Optimal Layout of CMOS Functional Arrays IC standard cell design.

Firstly, this topic is discuss about the Optimal Layout of CMOS Functional Array.

Optimal Layout is the layout of the arrangement of CMOS transistor with the implementation of a random logic function on an array of CMOS transistor.

After discussing about the introduction i.e. the basic of CMOS transistor, we will discuss how to create the Optimal Layout of CMOS Functional Array with the minimum separation based on euler path method.

INTRODUCTION

Designers of MOS LSI circuits can take advantage of complex functional cell in order to achieve better performance. This paper discusses the implementation of a random logic function on an array of CMOS transistors. A graph theoretical algorithm which minimizes the size of an array is presented. This method is useful for the design of cells used in conventional design automation systems.

In integrated circuit design it is possible to implement a logic function by means a circuit consisting of one or more elementary cells, such as NAND or NOR gates, or by means of a single functional cell. The basic advantages of functional cells, such as smaller size and better performance, are well known to designers of MOS LSI [1]. Theoretical results about network synthesis with complex functional cells have been reported in [2]-[4]. Some commercial products also take advantage of these properties [5]. However, most designers still use a limited library of cells. For example, NAND gates are often used as the only primitive cell. More details on the physical implementation of complex functional cells have been reported in [6]-[10]. Designers often have no confidence in the performance and merit of more complex