DESIGN AND ANALYSIS OF MULTIPLE PATHS TRACE BACK AND RECONSTRUCTION MODULE FOR DNA SEQUENCE ALIGNMENT ACCELERATOR USING ASIC DESIGN FLOW

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ABSTRACT

Bioinformatics is the analysis of biological information using computers and statistical techniques. Smith Waterman (S-W) algorithm for sequence alignment is one of the main tools of bioinformatics. It is used for searches and alignment of similarity sequence. This paper presents a novel approach and Analysis of Multiple Paths Trace Back and Reconstructions Module for DNA sequence alignment accelerator using ASIC design flow. The first objective is to construct the trace back and reconstruction module of the S-W algorithm with the multiple blocks and the functionality for each block. Second objective is to perform the timing analysis and third objective to implement the design using ASIC flow. The design was developed in VerilogHDL coding, simulated and synthesized using Xilinx ISE 12 and then re-implemented using Synopsys ASIC Tools implies the timing diagram and analyzes using the Design Compiler and Integrated circuit compiler to produce the layout. Resulted from Xilinx simulator and VCS expressed the output produced in single clock cycle for each blocks. As the conclusion the design is actually fully function for each block of Trace Back and Reconstruction.

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CHAPTER 1

INTRODUCTION

1.1 BACKGROUND OF STUDY

All the cells of an organism consist of some kind of genetic information and carried by a chemical known as the deoxyribonucleic acid (DNA) in the nucleus of the cell [1,2,3]. DNA is stored as a code made up of four chemical bases, which are adenine (A), guanine (G), cytosine (C) and thymine (T). Variations in our DNA sequences give us individual fingerprints, useful for identification and for the establishment of relationships. The use of DNA analysis as evidence in criminal trials is now well-established [4].

Cluster technique is one of the techniques for running sequencing analysis on a general purpose microprocessor, but it required more than one general purpose microprocessor [2]. By improving the cluster technique, the new parallelism with divide and conquer technique for Field Programmable Logic Array (FPGA) implementation was introduced [2].