CHARACTERIZATION AND FABRICATION OF 90nm PMOS WITH STRAINED SILICON USING SILVACO TCAD

This project is presented in fulfillment for award of the Bachelor of Electrical Engineering (Hons)

MOHD ARIFF BIN AB HAMID
2006130663
B. ENG (Hons.) ELECTRICAL
Faculty of Electrical Engineering
UNIVERSITI TEKNOLOGI MARA (UiTM)
Shah Alam, Selangor Darul Ehsan.

AKNOWLEDGEMENT

I am very greatly thanking the Glorious and merciful God for the wisdom and piece give me until I could finished this project. Without His bless this project might not complete on time.

My gratitude and appreciation also go to my supervisor, Dr. Fuziah Sulaiman for his precious ideas, guidance, suggestions and willing in sharing the knowledge towards the completion of this final project. I would also like to express my outmost

Special thanks to my lovely family and friends that support me throughout the process in completing this final project. Also thanks to everyone who has contributed either directly or indirectly throughout the thesis and this project.

ABSTRACT

This paper is looking into the enhancement of conventional 90nm PMOS by using graded silicon germanium layer (SiGe) within the channel and bulk of semiconductor.The performance of conventional 90nm PMOS and 90nm PMOS with silicon germanium layer was compared. A process simulation of Strained Silicon PMOS and its electrical characterization was done using TCAD tool. The analysis focused on Id-Vg, Id-Vd characteristic, and hole mobility changes. With the Germanium concentration of 35%, the threshold voltage Vt for the strained Si and conventional PMOS is -0.228035V and - 0.437378V respectively. This indicates that the strained silicon had lower power consumption. In addition, the output characteristics were also obtained for Strain Silicon PMOS which showed an improvement of drain current compared with conventional PMOS. The results were obtained from ATHENA and ATLAS simulator.

TABLE OF CONTENTS

DECLARATION i

ACKNOWLEDGEMENT ii

ABSTRACT iii

TABLE OF CONTENTS iv

LIST OF FIGURE vi

LIST OF TABLE vii

LIST OF ABBREVIATION viii

CHAPTER 1

INTRODUCTION

1.1 OVERVIEW 2

1.1.1 History of MOSFET 2

1.1.2 CMOS Nanometer Scaling 3

1.1.3 Strain Silicon 5

1.2 RESEARCH OBJECTIVES 7

CHAPTER 1

INTRODUCTION

1.1 OVERVIEW

Semiconductor industry experienced rapid development in the revolution of increasing density in a single chip. This revolution is leading by scaling the gate length and comply with Moore's law theory. While the predictions about the future development cause lot of novel technology being implant to the MOSFET to sustain its reliability. One of the novel strain is strain silicon CMOS that have been known to improve performance of CMOS. In this thesis is focused on improving performance by using SiGe layer on the channel PMOS.

1.1.1 History of MOSFET

Rapid scaling of MOSFETs drives increasing microprocessors performance and rapid growth of the information technology revolution. The underlying principle behind the revolution is Moore's law. In 1965, Gordon Moore observed that the number of transistors in a chip increased exponentially over time . Moore's law is possible because the transistor size decreases exponentially over time. When Moore made his prediction in 1965, transistor size was 100 m. During the last three decades, Moore's prediction has held as transistor size exponentially decreased from micrometers to submicrometers and then to deep submicrometers. Presently, with the introduction of 90-nm CMOS logic technologies and 45-nm transistors in 2003 , Moore's law is found to still be valid in the nanotechnology era. Fig. 1 shows the historical feature size reduction during the past three decades and the start of the nanotechnology era for the microelectronic industry as feature size moves from deep submicrometer to nanometer scale.