8T SRAM WITH DIFFERENT TYPE OF SENSE AMPLIFIER

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ABSTRACT

In this paper, it presents the 8T SRAM by using different type of sense amplifier which is voltage-mode sense amplifier (VMSA) and current-mode sense amplifier (CMSA) stored date. The objectives of this research is to identify which one of these sense amplifier has the most high speed, less delay, and low power dissipation and also has the smallest cell area in layout. Sense amplifiers are one of the most critical circuits in the periphery of CMOS memories. This plays an important role to reduce the overall sensing delay and voltage. Earlier voltage mode sense amplifiers are used to sense the date it sense the voltage difference at bit and bit lines bar but as the memory size increase the bit line and date line capacitances increases. The software that will use for simulation is SILVACO EDA which is Gateway and Expert for layout by using 0.18um technology. The results show that the CMSA has high speed which is has delay 36-46% performed better than VMSA, and low power dissipation is 5-15% compared to VMSA. But, VMSA has the better cell area where it has 31.50% smaller than CMSA and the DRC and LVS for both layouts is shows with no error and equivalent. All the objectives are achieved and it shows that the CMSA has more advantages compare to VMSA and it is suitable for high speed performance and low power circuitry.

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CHAPTER 1

INTRODUCTION

1.0 8T SRAM

Technology and supply voltage scaling continues to improve the logic circuit delay with each technology generation. However, the speed of the overall circuit is increasingly limited by the signal delay over long interconnects and heavily loaded bit-lines due to increased capacitance and resistance[1].

Static Random Access Memory (SRAM) is a type of semiconductor volatile memory (RAM) which keeps its data until the power is turns OFF. SRAM will store the binary logic bits '1' or '0'. It consists of an array of memory cells along with the row and column circuitry. SRAM has design to fill two needs that are to provide direct interface with CPU at speeds not achievable by DRAMs and to replace DRAMs in systems that require very low power consumption. The stability and area of SRAM need to be concern in designing SRAM cell. SRAM cell must be able to write and read data and keep it as long as the power is applied. The main challenge in designing SRAM cell is to ensure that the circuitry holding the state is weak enough to be overpowered during a write, and still strong enough to be not disturbed during read operation.

SRAM represents a large portion of the chip, and it is expected to increase in the future in both portable devices and high-performance processors. To achieve longer battery life and higher reliability for portable application, low-power SRAM array is a necessity [2].