

# **EFFECTS OF HIGH-K ON FINFET PERFORMANCE**

**This is presented in partial fulfillment for the award of the  
Bachelor of Engineering (Hons.) Electronic  
UNIVERSITI TEKNOLOGI MARA (UiTM)**



**FATIN SYAMILA BT. MOHAMMAD  
FACULTY OF ELECTRICAL ENGINEERING  
UNIVERSITI TEKNOLOGI MARA  
40450 SHAH ALAM,  
SELANGOR, MALAYSIA**

**JULY 2013**

## **ACKNOWLEDGEMENT**

In the name of Allah, The Most Generous and The Most Merciful. With the deepest sense of gratitude to Allah the Almighty for giving me strength and ability to complete my final year project and thesis.

My deepest gratitude is expressed to my supervisor, Suhana bt. Sulaiman, PTM (<http://ptm.asu.edu/>) for the SPICE model and the people from LTspice: LTspice/SwitcherCAD III - Groups - Yahoo! for all the guidance, support for all the guidance, support and advice provided to me throughout the final year project.

Last but not least, I also would like to express my appreciation to my beloved family, friends and anybody who are involved directly or indirectly for their support and devices during completing my final year project.

Thank you.

## ABSTRACT

Scaling down transistor to 45nm node and below might require new processing steps such as new gate stack or new device structure such as FinFET. Thus, in this work the use of high-k gate insulator - hafnium oxide ( $\text{HfO}_2$ ) on FinFET performance was investigated. SPICE model was used to describe the real device operation and designing a practical analog circuit for the AC analysis. Therefore, only the gate insulator is changed in the SPICE model from silicon oxide,  $\text{SiO}_2$  to  $\text{HfO}_2$  and the difference of the turn on current ( $I_{\text{ON}}$ ) is compared between planar and FinFET  $\text{SiO}_2$  gate insulator with  $\text{HfO}_2$  gate insulator FinFET transistor. The simulation results for 22nm node on inverter and chain inverter application show that better performance was obtained for FinFET compared to planar bulk CMOS.

## TABLE OF CONTENTS

CHAPTER	PAGE	
DECLARATION	i	
ACKNOWLEDGEMENT	ii	
ABSTRACT	iii	
TABLE OF CONTENTS	iv	
LIST OF FIGURES	vi	
LIST OF TABLES	vii	
LIST OF ABBREVIATION	viii	
CHAPTER 1	INTRODUCTION	1
1.0	BACKGROUND OF STUDY	1
1.1	PROBLEM STATEMENT	3
1.2	OBJECTIVE	4
1.3	SCOPE OF PROJECT	4
1.4	ORGANIZATION OF PROJECT	5
CHAPTER 2	LITERATURE REVIEW	6
2.0	INTRODUCTION	6
2.1	FINFET	7
	2.1.1 FINFET AND THE CHALLENGES	7
	2.1.2 FINFET: THE PROMISES	8
	2.1.3 HIGH-K MATERIAL: HAFNIUM OXIDE (HfO <sub>2</sub> )	9
2.2	PREVIOUS WORK ON FINFET AND HIGH-K	10
	2.2.1	10
	2.2.2	11
2.3	SUMMARY	12

# CHAPTER 1

## INTRODUCTION

### 1.0 BACKGROUND OF STUDY

Moore's Law (1965), states that the density of transistor and performance of chip will be double for approximately 18 months [1]. The phenomenon known as Moore's Law is then use as benchmark or describing the pace of evolution in the semiconductor world. After 50 years of Moore's Law the technology growth of integrated circuit is still increasing. As the dimension of a transistor shrank, the transistor become smaller, lighter, faster, consumed less power and in most cases was more reliable [2]. Nowadays, Jonathan Koomey, a professor from Standford University had come out with a new law which is named after his name, the Koomey's Law. As he presented for a historical analysis, that indicates the energy efficiency of computers, as measured in compute tasks per kilowatt, has doubled every 18 months throughout history [3]. The study notes that "significant new innovation" is needed for the law to hold in the future. These elements make transistor more desirable for new generation of computing technology in any category for fastest computers to smallest hand held devices.