Row Decoder and Row Driver Custom Design Using 0.18 μm CMOS Technology

This thesis is presented in partial fulfillment for the award of the

Bachelor of Electrical Engineering (Hons.) Electronic

UNIVERSITI TEKNOLOGI MARA (UiTM)

MD AIZUDDIN BIN ROSDAN
Faculty of Electrical Engineering
Universiti Teknologi Mara
40450 Shah Alam, Selangor Darul Ehsan
Malaysia

JANUARY 2013

ACKNOWLEDGEMENT

In the name of Allah S.W.T, The most gracious who has given me the strength and the guidance to completed this project. With the one and only Allah S.W.T as my guidance it is carried out smoothly.

I would also like to take this chance to give special thank to my supervisor throughout the entire two semester spans on the Final Year Project course which is Puan Suhana Sulaiman for her patience in guiding me with all the necessary sources to make my Final Year Project a success and also for all the knowledge that she conveyed on to me. Not forgot to my co-supervisor Dr. Azilah Saparon for her support and advises during the project.

Acknowledgements also are due to the lab technician which is Cik Ahmad Riduan that give me a permission to use the lab and give his full cooperation in completing the project. Thanks also given to my colleague for their comment and thought in any matter in the entire duration of Final Year Project course.

Finally thanks also to whom that is so many to mention that give their undying support and assist me in completing this project whether it is minor or major help. I am eternally indebted to my parents for their love, encouragement and support to completing this project.

ABSTRACT

This paper presents a design and analysis of row decoder and row driver used for 2KB content addressable SRAM memory. The decoder and driver were designed in a custom analog design and layout using EDA Tools Software with 180 nm technology library. The designed was focusing on optimizing the propagation delay and power consumption or dissipation because it is important to achieved fast SRAM transfer data with low power consumption. The row decoder and row driver was designed for 4-16 decoder using Pseudo NMOS. The finding reveals the improvement in propagation delay and power consumption or dissipation. From the finding, the propagation delay speed had improved by 21 ns to 6.18 ns and power dissipation had reduced from 600 mW to 177.54 μs. The simulation results was referred to the FairChild Semiconductor MM74HC154 datasheet for comparison. The power consumption for the decoder design using Pseudo NMOS also reduced compare to the NAND gate structure. The layout of overall designed have shown the layout versus schematic (LVS) results is equivalent and no error in design rule check (DRC).

TABLE OF CONTENTS

CHAPTER 1

INTRODUCTION

1.1 INTRODUCTION

Static random access memory (SRAM) stores the data bits in its memory as long as there is power supply. SRAM provides faster access to data and it is used for a computer cache memory. The SRAM access path is split into two portions, from address input to the row decoder and from row decoder to output read data path. An important part is the decoder which determines the section of memory cells that need to have a read (R) or write (W) performed on the memory cell. The inputs into the decoder is called the address, combined with the corresponding data coming from the bus into the SRAM are the elements that make up a port.

A memory device is a plurality of memory cells arranged in a matrix of rows and columns show in Figure 1.1. In order to access information in the memory cells, memory devices typically use a row address to indicate which row of memory cells the information can reside in. The output from the row driver is noted as row decoder driver that will be used to decode the row address and drive the wordline (WL) associated with the address. The row driver from the control logic affects the timing of the generation of WL signals because of propagation delay differences between the various rows based on their common control logic. When designing and specifying the memory device for timing, the worst case timing delay from the control logic to a row decode driver is determined and used for accessing information in the memory device.