Five-Phase Space Vector Modulation Voltage Source Inverter Using Large, Medium and Zero Vector Combination Technique

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Abstract –**The development of power electronics toward the future is massive and leads to the application of electric drives with the number of phase greater than three such as the multi-phase inverter. This research is about to generate five-phase AC voltage waveform from the five-phase space vector modulation VSI using the combination of active (large and medium) vector with zero vector switching technique and analyzed its result by implementing the switching technique into the simulation and hardware and record the performance of the output at the load. The Low Order Harmonic (LOH) such as 3rd, 5th and 7th harmonic produce by d3-q3 subspace will be reduce by using the combination of large, medium and zero vector technique**

Keyword – Space vector modulation, Voltage source inverter, active and zero vector.

I. INTRODUCTION

For a past few years ago, the industry back then applied the three-phase systems for the three-phase machinery for its uncomplicatedness [1,2]. To control the behaviour of the three-phase machinery, three-phase AC drives were used. On the other hand, since this drives for the three-phase machine used the power electronic converter for their supply, the number of phases for the machine was principally limitless [3]. Thus, a multiphase drives was introduced.

As the countless of research and development upon the making of power electronics and motor drives, it had unlocked the opportunity of discovering the Higher Phase Order (HPO) motors and drives [1]. This Higher Phase Order inverter or known as multiphase inverter had its own advantages over the three-phase inverter that are reducing the low-order harmonic and produce output voltage waveform that is near to the sinusoidal waveform [4].

For multiphase inverter, it will use the output of voltage source inverter as the main source to operate. In order to control the VSI, a certain number of Pulse Width Modulation (PWM) techniques were used. Nonetheless, a technique called the Space Vector Pulse Width Modulation (SVPWM) technique were introduced and was used rather than using the PWM technique. This is because SVPWM had the easiness of the digital implementation when compared to the PWM technique [3].

A. Past Study

In past research, there are several people that did research for five-phase voltage space vector modulation. Each of the research gives several results that will be stepping stone in doing this research for five-phase voltage VSI using the SVPWM. The result can be compared in Table I.

TABLE I
PAST RESEARCH ON FIVE-PHASE VSI USING SVPWM

Thesis	Research Result		
	3rd Harmonic	*5th Harmonic*	*7th Harmonic*
Paper [5]	17.9%	-	2.04%
	In this research, the large and medium space vector was applied by using the pre-defined zero space vector by having the positive time at zero space vector. This allowed the input vector reference can be wide-ranging from zero to maximum value that can be obtained.		
Paper [6]	28.908%	12.614%	4.825%
	This research had mention about the correlation of PWM carrier and SVPWM for five-phase VSI. This technique had been related to the harmonic injection in order to achieve higher output fundamental value. Thus, using combination of two large vector and zero vector was used		
Paper [7]	0.19%	0.01%	0.43%
	The large, medium and zero vector was been simulated and the data was recorded in this research. Comparing to the other two techniques, the THD for combination of large, medium and zero vector gives the lowest value.		

II. TWO-LEVEL FIVE-PHASE SVI

In two-level five-phase inverter, the number of semiconductor for switching purpose used is equal to 10, where the each upper and lower level got 5 semiconductors. This number of semiconductor use for switching can be related to m^n, where m would be the level of inverter that is 2, while n is the number of phase in the inverter that is 5. Thus, 2^5 , will be equal to 32 number of switching combination [1, 3, 5–7]. From this 32 switching, 30 are

active vectors (1-30), while the other 2 are zero vector (1 and 31) [1].

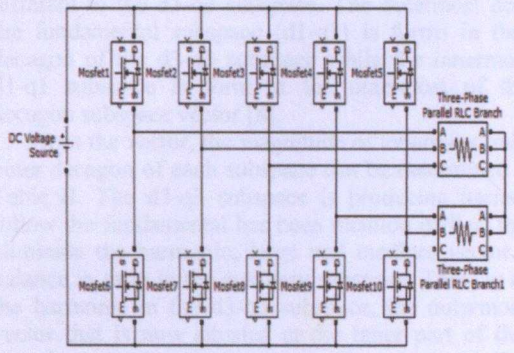


Figure 1: 5-Phase VSI

$$\left.\begin{array}{l} V_{xn}=\frac{4}{5}V_x-\frac{1}{5}\sum_{i,i\neq x}^{5}V_i \quad \text{if } x<5 \\ V_{xn}=\frac{4}{5}V_x-\frac{1}{5}\sum_{i,i\neq x}^{4}V_i \quad \text{if } x=5 \end{array}\right\} \quad (1)$$

Where,
x = (1,2,3,4,5)
V_{xn} = Phase-to-neutral voltage
V_x = pole voltage

From Figure 1, it can be seen that the construction of two-level five-phase VSI and it can be seen that each upper switches is connected series with the lower switches. From each point of switching in the vector, it contain five binary number from 00000 to 11111, where this binary had the connection to the level of the inverter. For binary '1', the upper switch will turn ON while binary '0', the upper switch will turn OFF. From the figure 1, connection of the output to the load is in star connection. At the output, the voltage-to-neutral for multiphase, that is for this study is five-phase VSI, it can be determined from the functions of leg voltage that can be referred to equation (1) [4, 8].

III. SVM FOR TWO-LEVEL FIVE-PHASE VSI

As the number of phase in the inverter had increased, using the space vector pulse width modulation (SVPWM) technique is the most preferred because it had the advantage of reducing the low order harmonic and also producing an output at its optimal over the three-phase technique [10]. As been mentioned earlier in the introduction, the number of switching combination of five-phase VSI is 32, that was obtained from 2^n, where 2 is the number of inverter level and n is the number of phase in the inverter [11].

$$\text{Number of subspace} = \frac{n-1}{2} \quad (2)$$

The subspaces for five-phase VSI can be calculated by referring to equation (2), where 2 subspaces that are fundamental subspaces (d1-q1) and auxiliary subspace (d3-q3) can be identified [9]. For both subspace, a vector of switching combination can produced for each of them as in Figure 2 and 3. In order to project switching combination for both subspace, they related to the equation (3) and (4).

$$V_{d1q1}=\frac{2}{5}V_{DC}\left[V_{an}+aV_{bn}+a^2V_{cn}+a^3V_{dn}+a^4V_{en}\right] (3)$$

$$V_{d3q3}=\frac{2}{5}V_{DC}\left[V_{an}+aV_{cn}+a^2V_{en}+a^3V_{bn}+a^4V_{dn}\right] (4)$$

Where:

$$a=\cos\frac{2\pi}{5}+j\sin\frac{2\pi}{5} \quad a^2=\cos\frac{4\pi}{5}+j\sin\frac{4\pi}{5}$$

$$a^3=\cos\frac{4\pi}{5}-j\sin\frac{4\pi}{5} \quad a^4=\cos\frac{2\pi}{5}-j\sin\frac{2\pi}{5}$$

By referring to Figure 2 and 3, the phase order for d3-q3 vector space is following the order of ACEBD instead of following the phase order for d1-q1 where the order of the vector are ABCDE. This is because the d3-q3 subspace follows the 3rd harmonic voltage system while the d1-q1 follows the fundamental voltage system [1].

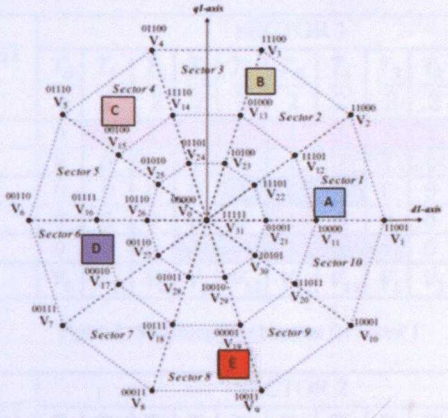


Figure 2: Switching Vector in d1-q1 Subspace [7]

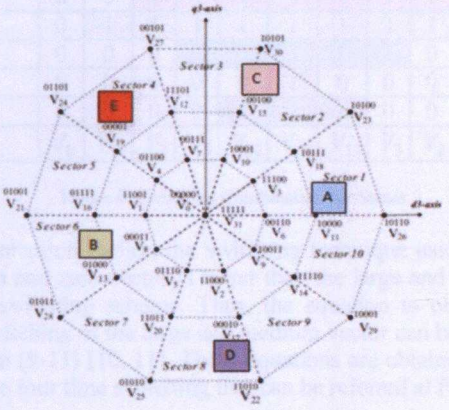


Figure 3: Switching Vector in d3-q3 Subspace [7]

By analysing on both vectors, it can be analysed that the coordinates of the switching vector for d1-q1 subspace is different to the d3-q3 subspace. The outermost decagon of the fundamental subspace (d1-q1) is forms in the middle decagon of the d3-q3 subspace while the innermost of the d1-q1 subspace is form at the outermost of the d3-q3 decagon subspace vector [8].

From the vector, the magnitude of innermost, middle and outer decagon of each subspace can be determined as in the Table II. The d3-q3 subspace is producing harmonic that follow the fundamental has been mention earlier. In order to eliminate the harmonic, large and medium vector must be balance in ratio in the auxiliary subspace. Thus, to eliminate the harmonic in the d3-q3 subspace, the outermost (large) vector that is now situated at the inner part of the vector, must be 1.618 longer than the medium vector [1,4]. In order to obtain the 1.618, the equation can be observed at equation (5-8). The example is based on using $V_2$and $V_{12}$where $V_2$is large vector while $V_{12}$is medium vector.

$$V_2T_2 + V_{12}T_{12} = 0 \quad (5)$$

$$-0.2472T_2 + 0.4T_{12} = 0 \quad (6)$$

$$\frac{T_2}{T_{12}} = \frac{V_{12}}{V_2} = \frac{0.4}{0.2472} \quad (7)$$

$$T_2 = 1.618T_{12} \quad (8)$$

In the vector, a one complete cycle of conduction angle is equal to 360° where each of the sectors had 36° conduction angle. For this study, the fundamental frequency to be applied is 50Hz. The time for one complete cycle is represent by $\frac{1}{(freq\ fundamental)}$,where it is equal to 0.02s or 20ms. Thus, for one sector to conduct, it will conduct for 2ms that is ($\frac{20ms}{10\ sector}$) [4].

TABLE II
MAGNITUDE FOR INNERMOST, MIDDLE AND OUTER VECTOR OF FIVE-PHASE VSI

Location	*Magnitude*
Innermost	0.2472
Middle	0.4
Outer	0.6472

IV. SWITCHING TECHNIQUE USING ACTIVE AND ZERO VECTOR

For large and medium switching technique, it is a technique that is greater than the large only technique. Large only just only used the outer part of the decagon in order to produce a switching combination.

This switching technique applied the zero vector schemes and combining it with the large and medium switching technique. By adding the zero vector, it will effect to the switching transition where only one switching is use in order to transition to other switching since it start and stop at zero vector ($V_0$and V_{31}) [7].This is lead to the improvement of producing low switching losses at the inverter.

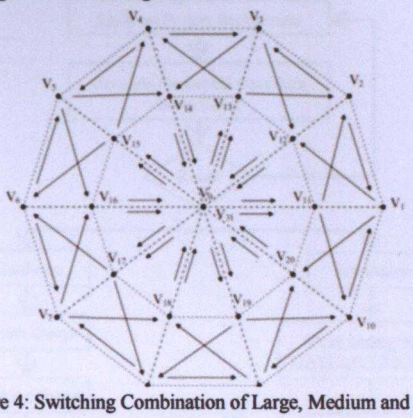


Figure 4: Switching Combination of Large, Medium and Zero Vector [7]

Figure 4 shows the combination of the large, medium and zero vector switching combination. From this vector diagram, ten sectors with a number of switching combination can be produce. This can be seen at Figure 5 and 6.

MOSFET	SECTOR 1										
	$\frac{T_0}{4}$	$\frac{T_1}{2}$	$\frac{T_2}{2}$	$\frac{T_3}{2}$	$\frac{T_4}{2}$	$\frac{T_0}{2}$	$\frac{T_4}{2}$	$\frac{T_3}{2}$	$\frac{T_2}{2}$	$\frac{T_1}{2}$	$\frac{T_0}{4}$
1	0	1	1	1	1	1	1	1	1	1	0
2	0	0	1	1	1	1	1	1	1	0	0
3	0	0	0	0	1	1	1	0	0	0	0
4	0	0	0	0	0	1	0	0	0	0	0
5	0	0	0	1	1	1	1	1	0	0	0
	V_0	V_{11}	V_2	V_1	V_{12}	V_{31}	V_{12}	V_1	V_2	V_{11}	V_0

Figure 5: Switching Combination for Sector 1

MOSFET	SECTOR 2										
	$\frac{T_0}{4}$	$\frac{T_4}{2}$	$\frac{T_3}{2}$	$\frac{T_2}{2}$	$\frac{T_1}{2}$	$\frac{T_0}{2}$	$\frac{T_1}{2}$	$\frac{T_2}{2}$	$\frac{T_3}{2}$	$\frac{T_4}{2}$	$\frac{T_0}{4}$
1	0	0	1	1	1	1	1	1	1	0	0
2	0	1	1	1	1	1	1	1	1	1	0
3	0	0	0	1	1	1	1	1	0	0	0
4	0	0	0	0	0	1	0	0	0	0	0
5	0	0	0	0	1	1	1	0	0	0	0
	V_0	V_{13}	V_2	V_3	V_{12}	V_{31}	V_{12}	V_3	V_2	V_{13}	V_0

Figure 6: Switching Combination for Sector 2

As mention earlier, the switching technique using large, medium and zero vector is better than the large and medium vector switching scheme. Thus, the equation to obtain the time switching of the large and medium vector can be seen at equation (9-11) [10, 11]. These equations are obtained based from the four time switching that can be referred at Figure 7.

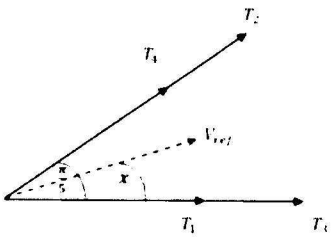


Figure 7: Switching Time on Each Sector [4]

$$T_a = M_a T_c sin((\ S\ x36°)\text{-}x) \quad (9)$$

$$T_b = M_a T_c sin(\ x\text{-}36°(\ S\text{-}1)) \quad (10)$$

Where,

S = sector M_a = modulation index

x = conduction angle T_c = carrier frequency

And from the above equation, it can obtain the four time switching equations that are:

$$\begin{aligned} T_1 &= T_a \left| \frac{V_{medium}}{V_{medium} + V_{large}} \right| \\ T_2 &= T_b \left| \frac{V_{large}}{V_{medium} + V_{large}} \right| \\ T_3 &= T_a \left| \frac{V_{large}}{V_{medium} + V_{large}} \right| \\ T_4 &= T_b \left| \frac{V_{medium}}{V_{medium} + V_{large}} \right| \end{aligned} \quad (11)$$

Because of this research is on active and zero vectors switching, addition timing switching was added in order to achieve these switching scheme. For the zero vector switching, T_0 is introduce. The equation of T_0 can be seen at equation (12).

$$T_0 = T_c - (T_1 + T_2 + T_3 + T_4) \quad (12)$$

V. METHODOLOGY

A. Flowchart

By referring to the flow chart in Figure 8, this research consists of several parts, namely:

1. Theoretical waveform
2. Simulation
3. Hardware

From the flow chart in Figure 8, the DSP act as a medium in order to run the code from the MATLAB/SIMULINK software and turn the digital signal into analog output signal so that the hardware can implement the SVM technique.

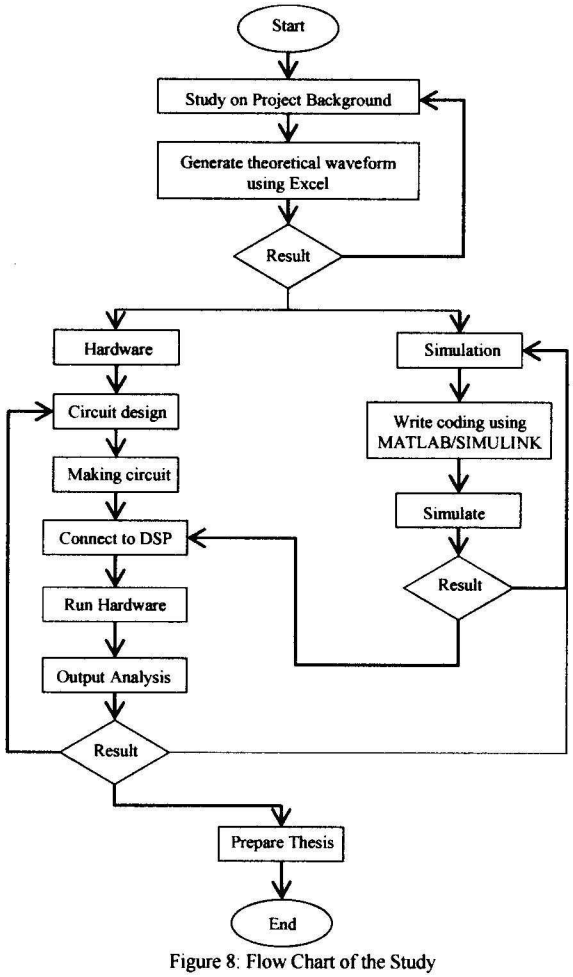


Figure 8: Flow Chart of the Study

B. Theoretical Waveforms

For theoretical waveform, Microsoft Excel was used in order to generate the graphical waveform by using the equation and input that had been determined in the study. This theoretical waveform will be a benchmark for the simulation and hardware waveform result.

C. Simulation

Before implemented the project into hardware, a simulation had been made using the MATLAB/SIMULINK by combining the coding of sector and switching sequence for the inverter and also block diagram that help producing PWM signal that follow the SVM method. In order to perform the simulation, the block diagram contains 3 parts that are:

1. Angle generating block
2. Coding block
3. Carrier frequency block

D. Hardware

There are 4 parts of in hardware that connected to each other as in Figure 9 such as:

1. DSP (ezdsp TMS320f2812)

2. Isolator circuit
3. Driver circuit
4. Five-phase inverter circuit

The ezDSP is a circuit that implemented the C coding that had been converted by the MATLAB using the real-time workshop and sent it to the DSP by using the Code Composer Studio.

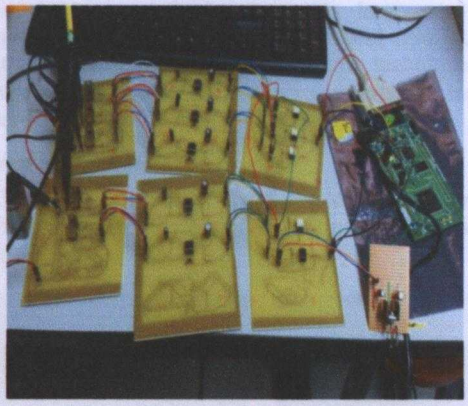


Figure 9: Complete Circuit of Five-Phase Inverter

The DSP is then linked to the isolator circuit that isolated the DSP circuit from the rest. The isolator circuit is used to protect the DSP from getting feedback of high voltage on the other circuit. The output of the DSP is send to opto-coupler so that the opto-coupler can send the DSP signal into the driver circuit.

The driver circuit is used in order to control the inverter input so that the inverter will operate according to the DSP signal. After the drive circuit, the last circuit which the inverter circuit, was the main part of the circuit in this research. This circuit will be used in order to produce AC output waveform that will trigger according to the timing set by the driver circuit.

VI. RESULT AND DISCUSSION

A. Simulation Result

The performance output of the waveform signal of the study is based on the setting given at Table III. The THD and Low Order harmonic of this research will be compare with the large only and large and medium THD.

TABLE III
VARIABLE FOR SIMULATION

Variable	*Value*
Frequency of fundamental, *f*	50Hz
Modulation index, Ma	0.8
Carrier Frequency, *fc*	1000Hz
Voltage supply, *Vs*	9V

By referring to the voltage waveform at figure 10, the complete cycle for each waveform followed the fundamental frequency that is 0.02ms. The output voltage for each waveform produce is 7.6V.

In order to analyse the performance of the switching using the large, medium and zero vector, the analysis on low-order harmonic had been made using the FFT analysis on the MATLAB/SIMULINK. This can be analysed as tabulated in Table IV, V and VI. The result obtains from the FFT analysis was compared with other FFT analysis result using large only and medium large switching method.

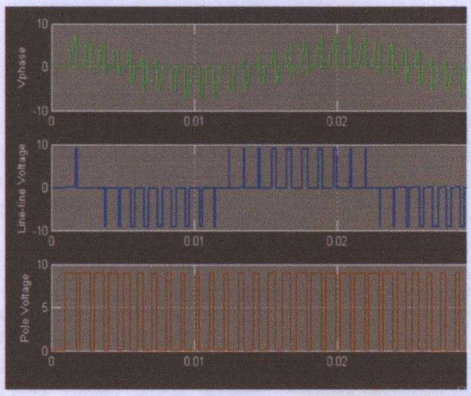


Figure 10: Output Waveform by using large, medium and zero vectors

TABLE IV
PHASE VOLTAGE RESULT FOR LOW-ORDER HARMONIC

SVPWM Technique	*Harmonic %*			
	3rd	*5th*	*7th*	*9th*
Large only	35.50	0.58	19.08	29.97
Large and Medium	10.35	0.91	2.02	0.9
Large, Medium and Zero	10.06	0.77	2.27	0.5

TABLE V
LINE-LINE VOLTAGE RESULT FOR LOW-ORDER HARMONIC

SVPWM Technique	*Harmonic %*			
	3rd	*5th*	*7th*	*9th*
Large only	55.67	1.70	28.46	29.35
Large and Medium	15.63	0.45	2.39	0.35
Large, Medium and Zero	15.09	0.34	2.59	0.27

TABLE VI
LINE-LINE VOLTAGE RESULT FOR LOW-ORDER HARMONIC

SVPWM Technique	*THD%*	
	Phase Voltage	*Line-Line Voltage*
Large only	81.87	65.18
Large and Medium	28.78	39.28
Large, Medium and Zero	28.66	38.83

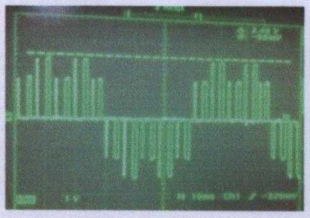
By analyse the result in Table IV and V, has been mentioned earlier, the Low Order Harmonic in large vector is the highest because it only use the outer vector only. The large and medium then reduced the low-order harmonic that

contained by the large only vector by maximized the switching technique into the medium vector. For large, medium and zero vectors, the low order harmonic is then further reduced because of lower switching loss from the switching sequence of the MOSFET in the inverter.

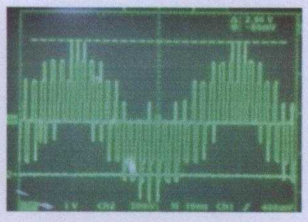
From table VI, the THD for the combination of large, medium and zero vector had the lowest value compare to other technique. By comparing the THD result to of the large medium and zero technique with large and medium technique, the THD of large, medium and zero technique is slightly lower than the large medium technique. This is because for large, medium and zero vectors, the harmonic is further reduced because of lower switching lost.

B. Hardware Result

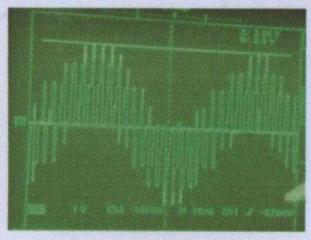
The waveform result from the circuit output will be compare with other switching technique. It can be analyse by referring to Figure 10.



(a) Large only Technique



(b) Large and Medium Technique



(c) Large, medium and Zero Technique

Figure 10: Phase voltage for five-phase using SVM technique

By referring to the output waveform at Figure 10 (a), the waveform produce is not following the sinusoidal output that is needed in the output. This is because, the switching timing combination of the large vector only used a small amount of vector switching situated in outermost layer of the decagon. By comparing figure 10(b) and 10(c), figure 10(c) is slightly smooth compare to figure 10(b). This is because, the zero vector utilise the switching technique by using only one switching for the transition from one sector to another sector.

VII. CONCLUSION

A research on the SVPWM for five-phase voltage source inverter using large, medium and zero vector switching is presented. By referring to the result obtain from the simulation and hardware, it can be conclude that the large, medium and zero vector switching is the best among the other switching technique because of its capability to maximise the usage of switching in order to reduce the harmonic that came from the losses in the switching technique. It also reduces the auxiliary subspace (d3-q3) that produce harmonic especially for the 3rd, 5th and 7th harmonic to the lowest possible by comparing the FFT generate with other two switching technique.

VIII. ACKNOWLEDGMENT

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