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PERFORMANCE ANALYSIS OF FULL ADDERS IN CIC DECIMATION FILTER

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Abstract

This article presents analysis of various full adder architecture on Cascaded Integrator-Comb (CIC) filter of delta-sigma ADC. The structure of CIC filter consists of an integrator and a differentiator stage that is built from a cascaded full adder and delay element. Since each of the element within CIC filter has its own low-power architecture, full adder is one of the block that consumes huge amount of power compared to others. In this paper, four different type of full adder's architecture is designed and simulated with CIC decimation filter. There are 28T conventional, pseudo-NMOS adder, 16T hybrid adder and modified 14T hybrid adder. The performance parameters such as delay, total power dissipation and power delay product (PDP) of CIC filter were compared. This analysis shows that 16T hybrid full adder CIC filter has reduced up to 38.15% of power consumption and 39.18% of power product delay compared to conventional adder. Hence, a complete 1-bit third order of 16T hybrid adder CIC filter is implemented with size area of 118.23µm × 22.38µm.

Keywords: Delta-sigma ADC, Low-power, CIC decimation filter, Full adder

1.0 INTRODUCTION

In accordance with advance technology, Internet of Things (IoT) has become one of the major focus on upcoming devices. Today, IoT has become essential features in major electronic devices such as smartphone, wearable device, sensor and etc. In these IoT devices, analog to digital converter (ADCs) are required to convert real time analog signal to digital signal for algorithm process. Furthermore, ADC in IoT devices demand a range of requirements from medium to low speed, less complexity, high resolution and low power for digital signal processing applications (Liu, Furth, & Tang, 2015). Besides, the size of ADC also become important in order to pace up with shrinking size of devices.

In conventional ADC, the sampling rate of the ADC are adhered to Nyquist sampling theorem which a signal must sampled at least twice of the highest signal frequency. Nyquist ADCs have the relationship as shown in equation below.

$$f_B < 0.5 f_s \quad (1)$$

where f_B is the bandwidth frequency of input signal and f_s is sampling frequency.

$$f_S = K \times 2 f_B \quad (2)$$

where K is defined as oversampling ratio.

In the other hand, oversampling ADCs usually have K times of sampling frequency larger than signal frequency. Due to high sampling rate, oversampling converters can achieve higher resolution and able to tolerate with analog signal imperfections (Sohel, Reddy, & Sattar, 2012).

Delta-sigma ADC is a converter works under delta-sigma modulation. Delta-sigma modulation sample the input signal at high oversampling rate up to few megahertz to reduce aliasing noise and phase distortion. During modulation process, lots of quantization noise will occurs at output signal spectrum. However, if we increase the sampling frequency to a very high spectrum, majority of quantization noise will be shifted to higher frequency range. Then, the quantization noise can be eliminated by passing a low pass filter. Therefore, a typical delta-sigma ADC consists of two main blocks which are modulator and decimation filter as shown in Figure 1.

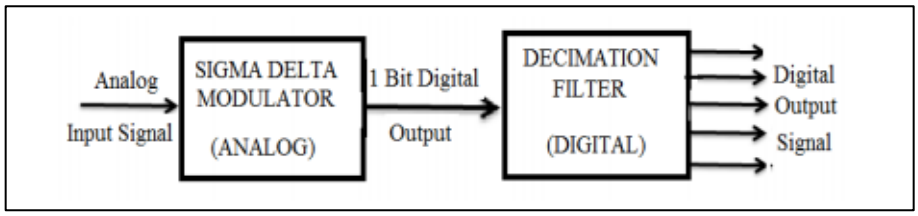

Figure 1 Delta-sigma ADC block diagram (Sohel, Reddy, & Sattar, 2012)

In modulator, analog signal as input are encoded to 1-bit stream digital signal. Then, decimation filter converts 1-bit stream signal to digital output with higher resolution (Moses, 2015). Decimation filter also acted as a low pass filter to remove quantization noise at higher spectrum. Besides, decimation filter also known as down sampler which the clock frequency is reduced to produce normal rate output signal.

In (Hogenauer, 1981), a multiplier-less cascaded integrator-comb (CIC) filter is introduced by Eugene Hogenauer. In this CIC filter, there are two main stages which are integrator and differentiator. It can be used as decimation and interpolation filter by swapping the arrangement of integrator and differentiator. CIC filter could be constructed by using delay element and full adder. Hence, CIC filter is widely used due to its low complexity of the circuit compared to conventional finite impulse response (FIR) decimation filter.

This work is presented using different architecture of low power full adders to construct a complete CIC decimation filter. A low power 1-bit 3rd order CIC filter was realized by using 130nm CMOS technology in Mentor Graphic. The next section describes the CIC filter's architecture and filter parameters. Section III presenting different type of 1-bit full adders. The simulation result and comparison table of delay, average power and PDP are presented in Section IV. Thus, last section concludes the work.

2.0 CIC DECIMATION FILTER ARCHITECTURE

In this section, a cascaded integrator-comb filter is designed as decimation filter based on (Hogenauer, 1981). The main stages of the CIC decimation filter are integrator stage and comb stage. N-order of multistage CIC decimation filter will have N number of integrator and comb stages. However, the number of order of CIC filter must at least one order higher than delta-sigma modulator. The relationship of number of orders of CIC filter and its modulator is as following:

$$\boldsymbol{N > \Delta\sum_{order} + 1} \tag{3}$$

where N is number of stages of CIC filter and $\Delta\sum_{order}$ is order number of modulator.

If $\boldsymbol{B_{in}}$ is the size of input stream from modulator, the output word size, $\boldsymbol{B_{out}}$ can be calculated as below.

$$\boldsymbol{B_{out} = N \log_2 RM + B_{in} + 1\ sign\ bit} \tag{4}$$

where R is decimation factor and M is differential delay that usually limited to 1 or 2.

The modulator output bit is always straight binary signal where $\boldsymbol{B_{in}}$ is 1 bit. Therefore, CIC filter operation is done in 2's complement **(Loloee)**. A coder circuit is required to convert modulator output to 2's complement form before being passed to CIC filter.

2.1 Integrator Stage

Basically, one order of integrator stage consists of a full adder followed by a delay element in feedback loop. Delay element can be constructed by a simple register such as flip flop or latch. During integrator stage, the low pass filtration is done to 1-bit stream input signal. The integrator stages are clocked with oversampling frequency, f_S as shown in Equation 2. The block diagram and circuit architecture of first order integrator stage are shown in Figure 2.

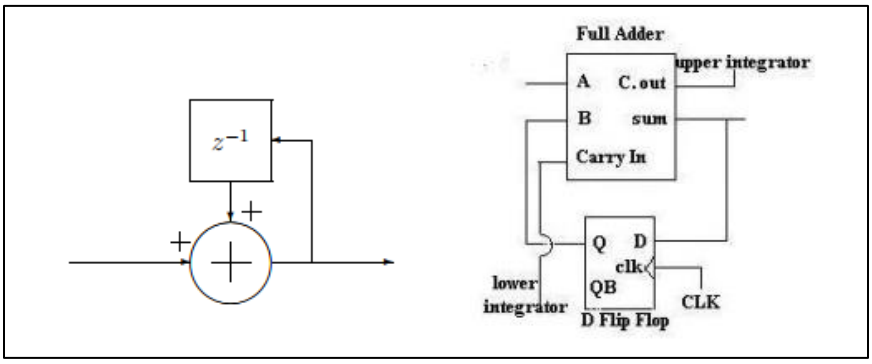

Figure 2 Block diagram of integrator & structure of integrator (Loloee)

2.2 Differentiator Stage

For decimation filter, the integrator stages are followed by Nth stage of differentiator. Differentiator stage's function as old symmetric FIR filter (Sohel, Reddy, & Sattar, 2012). The 1-bit stream passed down from integrator are computed by summation. The summation is done between integrator output and delay clocked at $\boldsymbol{f_s/R}$. In order to reduce output signal to Nyquist rate, the oversampled signal from integrator is being factor down by R at this stage. The basic structure of differentiator is shown in Figure 3.

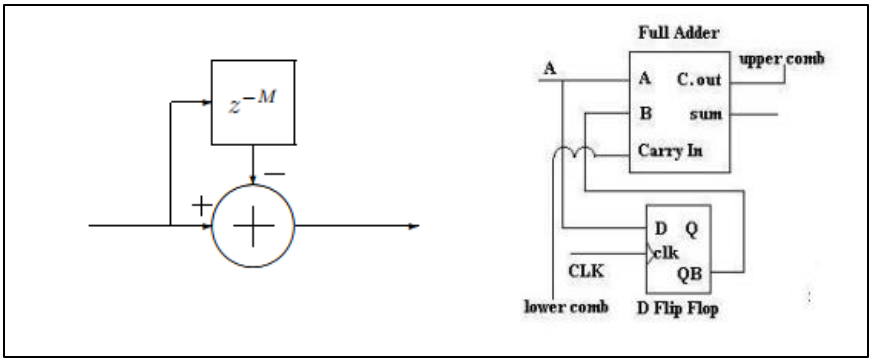

Figure 3 Block diagram of comb & structure of comb (Loloee)

2.3 Overall CIC Decimation Filter

As mentioned in (Hogenauer, 1981), Nth order of decimation filter consists of N stage of integrator and differentiator. In this case, 3rd order of CIC filter constructed from 3 stages of integrator cascaded with 3 stages of differentiator as in Figure 4.

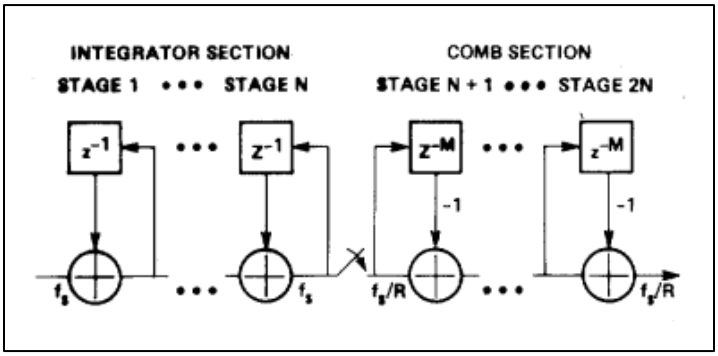

Figure 4 CIC decimation filter (Hogenauer, 1981)

Delay elements in integrator and differentiator are used to propagate input signal to delay one clock cycle. In this paper, the effect of delay element on CIC filter is not analyzed for performance analysis. Therefore, a conventional delay flip flop is used to trigger signal when the clock is positive-edged triggered. A 1-bit 3rd order CIC decimation filter is designed based on specification as Table 1.

Table 1 Design Parameter of CIC Filter

Aspect	Value
Number of Order, N	3rd order
Sampling frequency, f_S	2.56MHz
Decimation factor, R	64
Output freqency, f_{out}	40kHz
Total output word, B_{out}	20 bits

3.0 CIRCUIT DESIGN FOR FULL ADDER

The main focus of this work was to perform analysis on low power full adder of CIC filter. Full adders are required to do summation of digital signal. To achieve lowest power consumption of CIC filter, there are several architectures of CIC filter. In (Hurrah, Jan, Bhardwaj, Parah, & Pandit, 2015), the non-recursive comb filter has proved that it required the least power consumption. The architecture of low power design of CIC filter become a bottleneck for further reduction of average power dissipation. Therefore, a small amount of power reduction in full adder architecture will become significant for entire CIC filter. For this work, a 1-bit 3rd order of CIC filter contains 6 full adder blocks and it easily up increases to 60 units of full adder if a 20 bits CIC is being designed.

3.1 Conventional 28T Full Adder

Full adders of CIC filter are using single bit static CMOS logic styles. According to (Chauhan & Sharma, 2016), conventional CMOS full adder has relatively low average power consumption in 180nm and 90nm CMOS technology. Conventional full adder also has lower delay if set side by side to other common structure such as complementary pass transistor (CPL) adder, transmission adder (TFA) and transmission gate adder (TGA). The drawback of conventional full adder is larger area as it is made up of 28 transistors. Figure 5 shown the static complementary full adder structure.

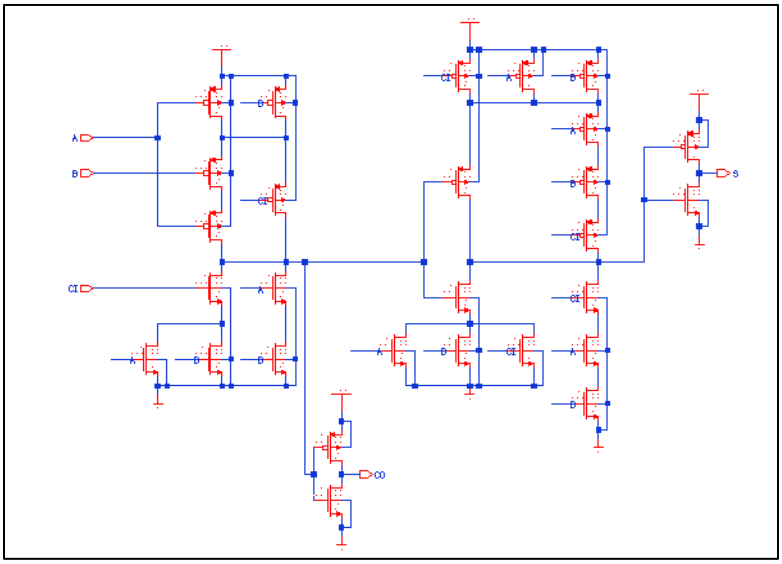

Figure 5 28T conventional full adder schematic

3.2 Pseudo NMOS Full Adder

Static complementary CMOS style adder consists of pull down and pull up network. In Figure 6, pseudo NMOS technique is used to replace the pull up network with single PMOS and permanently grounding the gate terminal. In this architecture, the pseudo NMOS adder can achieve higher speed and lower transistor count (Rao.Ijjada, Ayyanna.G, Reddy, & Rao, 2011).

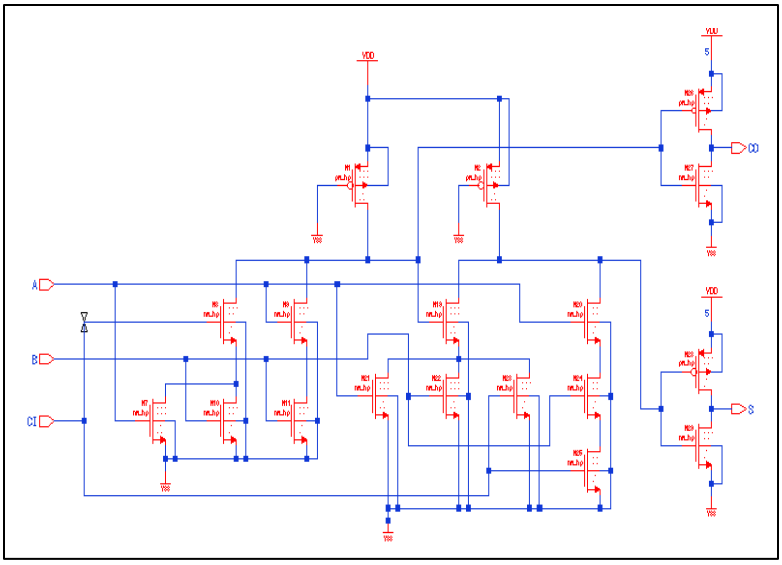

Figure 6 Pseudo-NMOS adder schematic

3.3 Hybrid Full Adder

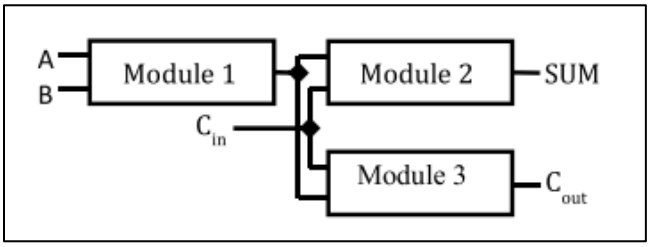

Figure 7 Hybrid adder's schematic structure

Hybrid adders are another novel architecture for low power and area efficiency design. The hybrid adder can be represented by 3 modules as shown in Figure 7. Module 1 and module 2 are XNOR modules to perform summation (SUM) of input signal A and B. Module 3 generates the output carry signal (C_{out}). The advantage of hybrid adder is each individual module can be modified to achieve better performance in term of power, delay and area.

As Figure 8, 16T hybrid full adder has showed that average power decreases greatly compared to conventional full adder (Bhattacharyya, Kundu, Ghosh, Kumar, & Dandapat, 2015)The propagation delays also improved due to fewer number of transistors. In Figure 9, one example of modified architecture of module 1 for hybrid adder is done to reduce 2 transistors from previous architecture. The modified 14T hybrid full adder roughly cut down half of the power dissipation, delay and PDP against 16T hybrid adder (Kumar & Srikanth, 2015**)**.

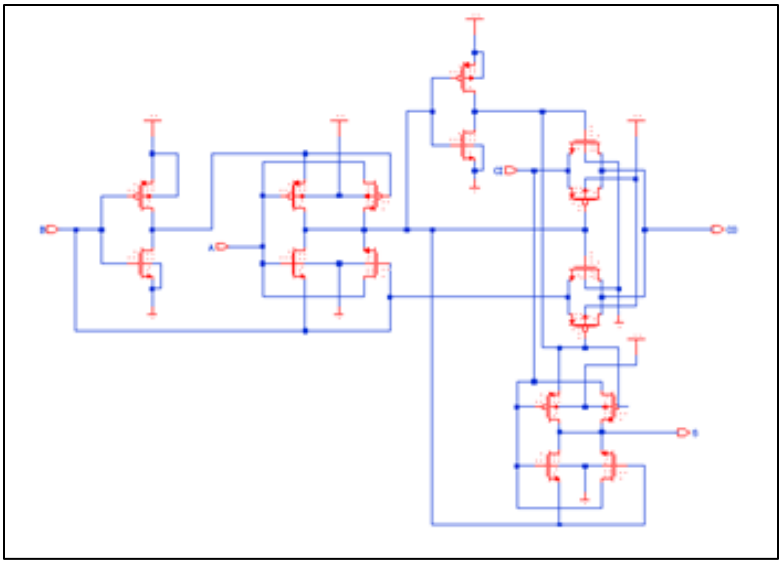

Figure 8 16T hybrid full adder schematic

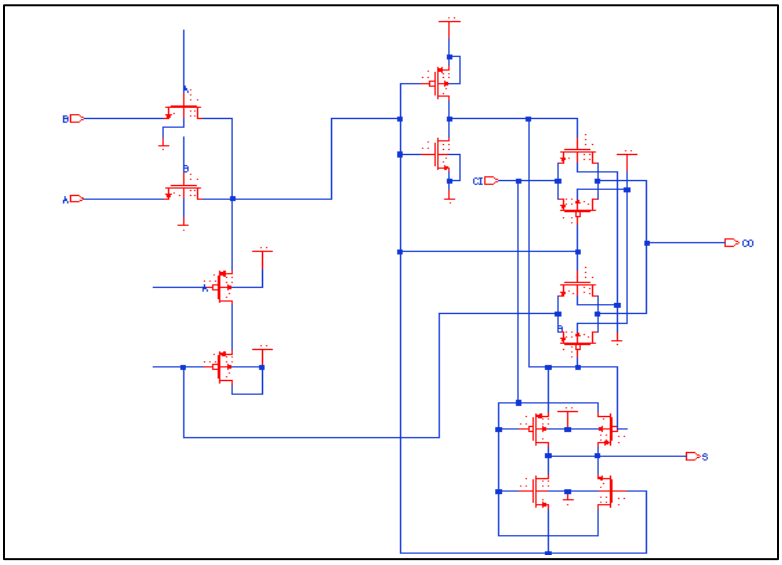

Figure 9 14T modified hybrid full adder schematic

In previous work, the full adders are simulated individually in 130nm or 180nm CMOS technology. However, the performance of these adders does not justify that they can perform similarly when integrated within CIC filter. The full adder performance in CIC filter depends on various factors to maintain a stable operation. The propagation delay and leakage current in CMOS transistor will cause large amount of power. These four type of 1-bit full adder architecture have been simulated together with CIC filter to study their performances.

4.0 SIMULATION RESULTS

All designs were implemented in 130nm CMOS technology using Mentor Graphic tool. The CIC filter with different full adder architecture are supplied with equivalent parameters in Table 1. The design of CIC filter is then simulated in various of supply voltage (VDD) from 1.0V to 1.4V. Pre-layout simulation results of all designs were compared in term of average power consumption, propagation delay and power-delay product (PDP) in Table 2-4.

Table 2 Simulation results for CIC filter at 1.0V

VDD	1.0V		
	P,ave (nW)	**Delay (ns)**	**PDP (fJ)**
CCMOS	20.2067	52.1691	1.0542
Pseudo MMOS	380.0865	72.3111	27.4845
Modified 14T Hybrid	22.5465	52.9245	1.1933
16T Hybrid	14.5086	31.2761	0.4538

Table 3 Simulation results for CIC filter at 1.2V

VDD	1.2V		
	P,ave (nW)	**Delay (ns)**	**PDP (fJ)**
CCMOS	34.146	4.8499	0.1656
Pseudo MMOS	783.729	6.1083	4.7873
Modified 14T Hybrid	70.5793	4.2633	0.3009
16T Hybrid	24.665	4.0409	0.0997

Table 4 Simulation results for CIC filter at 1.4V

VDD	1.4V		
	P,ave (nW)	**Delay (ns)**	**PDP (fJ)**
CCMOS	70.7032	2.8299	0.2001
Pseudo MMOS	969.4312	2.9871	2.8958
Modified 14T Hybrid	129.3593	2.7584	0.3568
16T Hybrid	43.7314	2.7828	0.1217

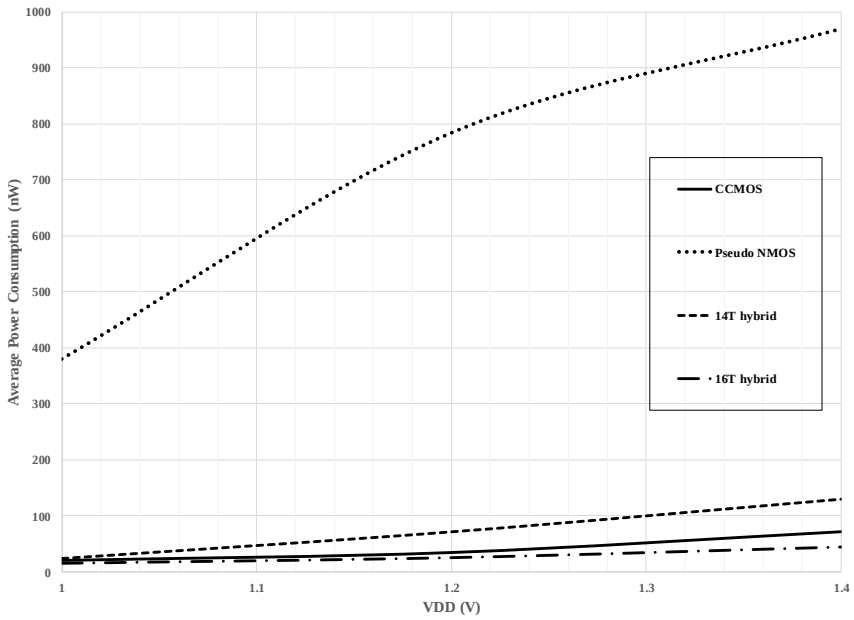

Figure 10 Comparison of power consumption of various full adder in CIC filter

At 1.0V supplied voltage, 16T hybrid full adder integrated within CIC filter has attained the lowest power consumption compared to others. From Figure 10, cascaded 14T hybrid adder CIC filter has lowest power consumption when peak input voltage applied from 1.0V to 1.4V. Delay of CIC filter increases when the applied voltage decreases because logic gate speed faster in higher voltage. Since, 16T hybrid full adder achieve the target of lowest power dissipation at 1.0V, the design has been implemented in layout shown in Figure 11 & Figure 12. The total layout area of 1-bit 3rd order CIC filter is 118.23µm × 22.38µm.

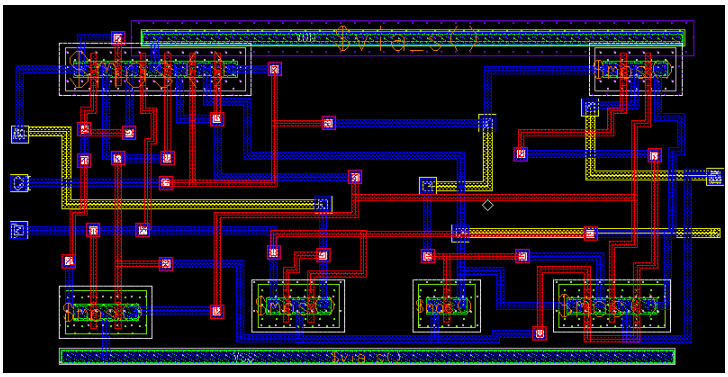

Figure 11 16T hybrid full adder layout

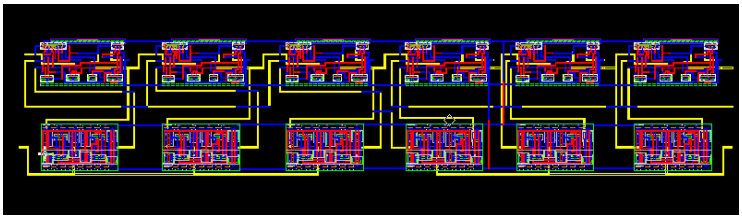

Figure 12 CIC decimation filter with 16T hybrid adder layout

5.0 CONCLUSION AND FUTURE WORKS

In this work, a basic 1-bit CIC decimation filter has been constructed and design extended to 3rd order of single bit CIC filter. The simulations are carried out on 130nm CMOS technology by using Mentor Graphics tools. The standard design of filter is then approached with 4 various low-power full adders: CCMOS, Pseudo-NMOS, 16T hybrid and 14T modified hybrid adder. The simulation results show that low power architecture of full adder gives relatively reduction in power consumption and area efficiency when cascaded into CIC filter. The 1-bit of 3rd order CIC decimation filter integrated with 16T full adder has achieved lowest power consumption and PDP at 1.0V. The 16T hybrid adder has achieved 38.15% of power reduction and 39.18% of PDP reduction compared to conventional full adder.

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