FPGA On-Board Memory Studies and Performance Analysis

Muhamad Aiman Bin Muhamad Aznan
Faculty of Electrical Engineering
Universiti Teknologi MARA
40450 Shah Alam, Selangor, Malaysia
aimanaznan15@gmail.com

***Abstract* – This paper present Field Programmable Gates Array (FPGA) on-board memory studies and performance analysis by designing a controller of memory using Verilog code. Inside this type of FPGA board, there are three types of on-chips memory available that is SRAM, SDRAM and FLASH memory. The memories have its own capability and function. The purpose of this study is to determine the performance for each types of memory in term of its area and power. This study is expected to help students in the future to fully understand on board memory. This study achieved by design controller using Verilog code on FPGA board and test the output through seven segment displays. Quartus tools as a software to compile Verilog code. Then, Timing Analyzer and Power Tools used to obtain the area and power consumption. From the analysis, SDRAM has maximum area with 89 logics then follow by SRAM with 88 logic and last is flash with 83 logics. For power consumption, SDRAM is lower follow with flash then SRAM is higher power consumption. All the memory successfully obtained its performance as expected.**

Keywords; Memory Performance, Area, Power, Memory Controller

I. INTRODUCTION

Memory is an important component inside the computer itself. It has information capability to store data either temporary or permanently and widely used in processor architecture. Although previous studies stated the performance is not enough to optimize the memory performance due to the long memory access potential[1]. For information, memory is divided into two types on memory that is volatile memory and non-volatile memory. Random Access Memory RAM is known as one of the volatile memory. Volatile memory is a type loses its content when the computer or hardware device loses power[2]. While non-volatile memory will save it content even the device loses power[2] . Non-volatile memory is expected to enrich the next generation computer system[3].

Why memory is important to the computer or hardware? This is because the speed is different when compared to all device in computer or hardware. RAM have two types that is SRAM and SDRAM. While SDRAM have many level, the latest one is DDR4 ram. Because the DDR is a very low cost then is widely used to custom own computer where they are usually used to run the functions of storage[4].

This project is to studies and analyse memories performance on the FPGA board. The performance such as area and power be obtained by designing controller using Verilog code. Result was collected through Quartus software. Inside Quartus itself, it has Timing Analyzer, Power Tools, and Fitter to check the power, and area. The controller also tested on the FPGA board. Specific FGPA board that used is Altera DE2-115 to run this project. The main purpose of this project is to facilitate to future students to make reference. This is because there is lack of study in details about the memory on chip performance and all the information can be used for future student as their reference.

FPGA are available in a varied range of sizes with the dissimilar feature. In other words, each of the various board has a different array of feature. FPGA and ASIC are needed each other to create hardware to be more effective[5]. It also is widely used because can operate at high-speed performances in a moderately minimal footprint[6]. SRAM, SDRAM and FLASH memories is built-in on the FPGA board. Furthermore, all memories type on the FPGA board have their own performance, speed and power.

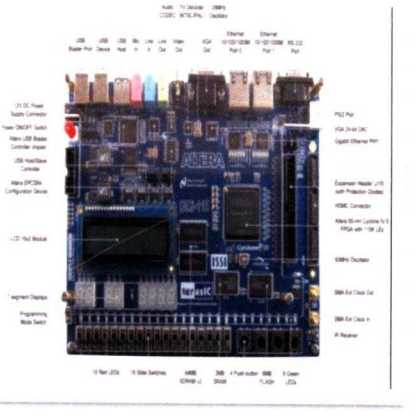

Fig.1. FPGA board Altera DE-115 (Cyclone IV) [7]

For information, on the FPGA board contain SRAM, SDRAM and FLASH memory. The data was recorded by comparing all these memory in term of their performance. Performance of the memories has been measured by designing a memory controller. SRAM, SDRAM, and FLASH memory has different controller design and the coding will implement to the FPGA board.

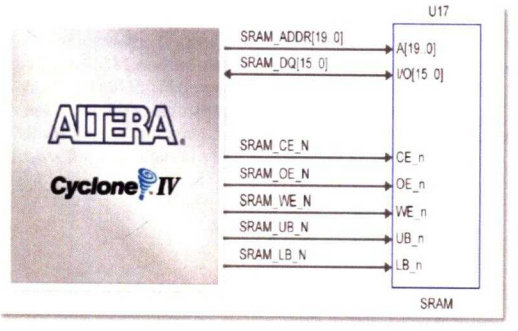

Fig.2. SRAM architecture connection between processor[7]

SRAM is the chip programming built by ram that hold data in a static form as long as the memory has power[8]. This called volatile type memory. In term of speed DRAM is slower than SRAM but SRAM is more expensive to construct because of complex circuit[2]. SRAM contains 2 MB memories with 16-bit data width. The configuration of the design in the FPGA chip is stored in SRAM cells and have maximum performance of frequency about 125 MHZ under standard 3.3v[9]. Others data also collected from other studies related to SRAM memory. For example, according to research article, the area that used for SRAM memory is 4.984 µm and the power is 560 nW[10].

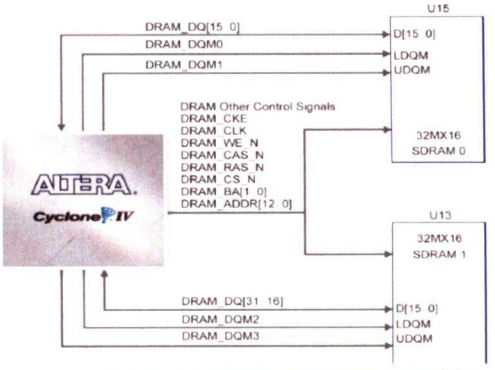

Fig.3. SDRAM architecture connection between processor[7]

SDRAM is another type of volatile memory. SDRAM must be refreshed periodically to maintain its content. The architecture of SDRAM is much smaller than SRAM. It widely used in memory circuits because it is one of the most capable solutions for achieving a higher data and can reduce the signal voltage swing[11]. SDRAM divides up its memory space into banks, rows and columns [7]. Contains 128 MB of SDRAM and using two 64 MB SDRAM devices, each consist separate 16-bit data lines. Use 3.3V LVCMOS signalling standard [9]. Others studies stated that the area / the overall number of logic cell altera design is 309[12]. While others paper records that the power dissipation for SDRAM memory is 2.436 µm[13].

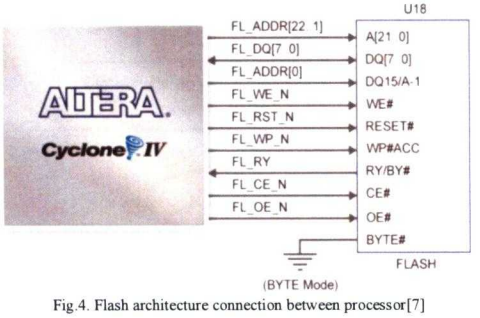

Fig.4. Flash architecture connection between processor[7]

FLASH memory is a non-volatile type used frequently in embedded system, retains its content after power is off. The FLASH memory has a have same address and data bus. Instead, it uses a serial programming scheme that transferring the data[2]. Before flash memory can be written, it must be erased. This memory assembled with 8 MB of FLASH memory using an 8-bit data bus. It uses 3.3V CMOS signalling standard. Usually used for storing software binaries, images, sound or others media[14]. According to others study, the area / total number of logic cell for FLASH memory is 197[15].

I. METHODOLOGY

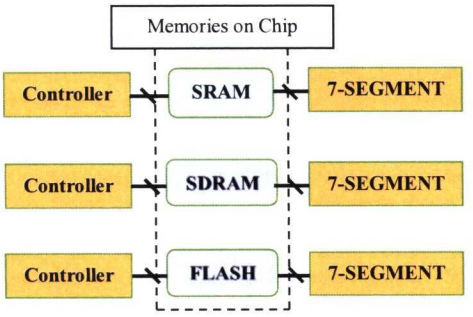

Fig.5. Block diagram of memories

Figure above shows the block diagram of methodology. A controller was design to control the memory on FPGA board. This project used Altera DE2-115 with Cyclone IV E to test the controller. In addition, on this FPGA board contain memories of 2MB of SRAM, Two 64MB SDRAM and 8MB of Flash memory. Verilog code is used to design the controller and the code was compile on the Quartus software. The main idea of Verilog code is same but difference in term of assigning the pin of all the memories itself. Lists of the pin are guide on the Altera DE2-115 user manual. As mention above, SRAM memory have 2MB with 16-bit data bus and contains 20 of address. SDRAM memory have 128MB using two 64MB and each device consists of separate 16-bit data bus and contains 13 of address. Flash memory have 8MB using 8-bit data bus and contains 23 of address.

Quartus tools has been used to compile the Verilog code and implement the code to the FPGA board as a controller for each memory. In the Quartus software, there has Timing Analyzer and Power Tools to obtain the area and power of the memories. To test the functionality of controller on the FPGA board is by using the switch as an input and 7 segments as an output. A text file that contain address data has been add to display the result. There are 16 data from text file with different address in hexadecimal format. The process of controller is read and write the data from text file and display to the 7-segment. An input from switch is write to the memories either SRAM, SDRAM or FLASH and read back with display the sequence and the correct data addresses from text file after the clock is trigger.

Lastly, all controller of the memories was simulated using simulation waveform editor under university program in Quartus software. This method is to check the functionally of the memory controller. Input from switch counted from 0000 to 1111 and the output from sram_dq can be seen based on input value. The seven segments also checked for every hex. The changing of high and low condition for every hex from seven segments is generate base on output data at waveform simulation.

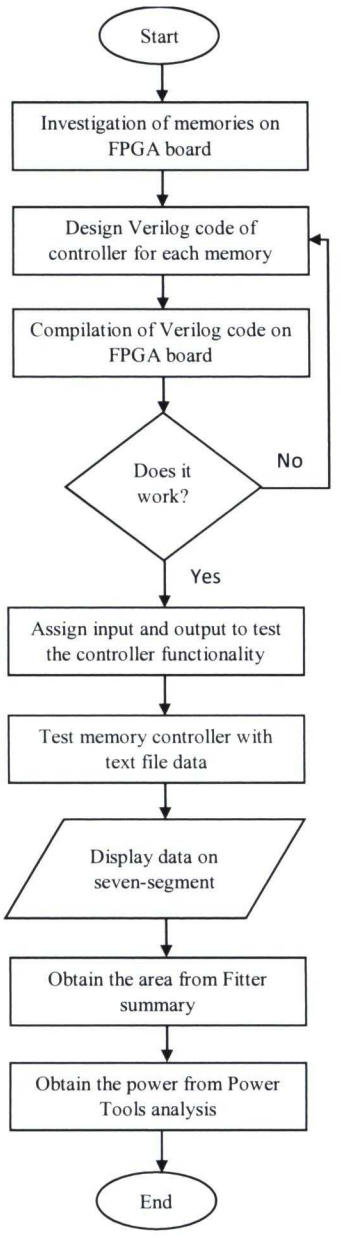

Fig.6. Flowchart of the project

Investigation of memories on FPGA Board by do a research about FPGA board architecture and find available memories on the board. In this section, all of the theory about memories that related to this project is list down as a reference. Source can be found on journal, website, books and datasheet of board itself. In addition, design Verilog code of memory controller by designing the software of the project. Since this project is to studies memory on FPGA board. The software design is in Verilog to control the memories. The main of Verilog controller is same but different assigning the pin that depend on memory either SRAM, SDRAM or FLASH. After designing process was completed, compile the program code in Quartus software without any errors. If there any errors than troubleshoot the design controller until the problem solve. Proceed to assigning switch as an input and seven segments as an output to display the result functionality of controller. The controller has been tested on FPGA board by using text file. Text file contains 16 addresses in hexadecimal as shows in the result table below. An input from switch act a binary number that determine the sequential of addresses in the text file. As an output, seven segments of HEX0 to HEX3 reserved to display output data and HEX4 and HEX5 display the address of output data from text file. For example, toggle switch is all low '0000' then the address '0' and output data is '0152' display from seven segments. Obtain the area and power consumption by using Fitter summary and Power Tools analysis. After complete the compilation for each memory controller, expand fitter summary to obtain the number of logic gate was used for each memory types. For power, use Power Tools analysis that are provided in Quartus software.

I. RESULT AND DISCUSSION

A. Waveform

i. SRAM

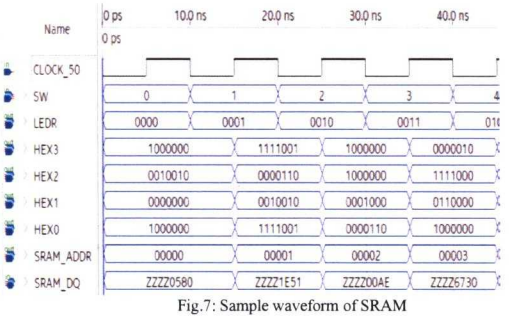

Fig.7: Sample waveform of SRAM

Figure above shows the waveform of SRAM memory. This waveform generated using 'Simulation Waveform Editor' that provided in Quartus software. Input and output was simulated to check the functionality of the memory controller. Switch as an input contain 4-bit that is from '0000' to '1111'. Hex0 to hex3 show the output from seven segments in binary radix. 'Sram_addr' count the address from text file while 'sram_dq' display the data from text file depend on the input switch. Below is the example of seven segment from address '0F'.

TABLE 1. Example of 7-segments of SRAM from address '0f'

HEX	Binary	7-segments display
HEX3	1000000	
HEX2	0010010	
HEX1	0000000	
HEX0	1000000	

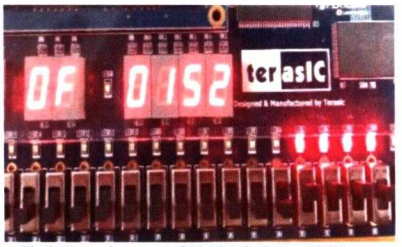

Fig.8: Example output of SRAM display on FPGA

In the figure 8 is the example of one of the output display from seven segments on FPGA board of SRAM controller. Input from switch '1111' provide data from text file of the address '0F' that contains data '0580'. The following data tabulate in the table below:

TABLE 2. Output data tabulated from SRAM

Switch	Address(Hex)	Output(Hex)
0000	00	0580
0001	01	1E51
0010	02	00AE
0011	03	6730
0100	04	0205
0101	05	8056
0110	06	FFEA
0111	07	0450
1000	08	02DA
1001	09	1890
1010	0A	0576
1011	0B	D20A
1100	0C	0125
1101	0D	018E
1110	0E	00FF
1111	0F	0152

Table above are the result from the of SRAM controller. All input was simulated on Quartus software and tested on FPGA board. The input switch is same to the address because it represents the sequence of data from text file. The result from both method is true when compare to the data in the text file. This can be assumed the SRAM controller is work well.

i. SDRAM

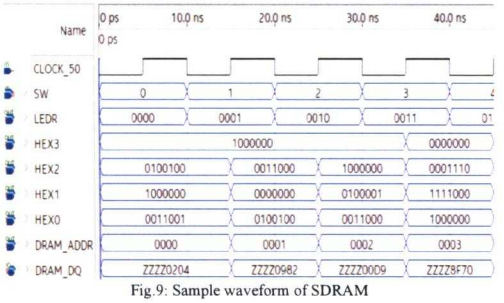

Fig.9: Sample waveform of SDRAM

Figure above shows the waveform of SDRAM memory. 'Sdram_addr' count the address from text file while 'sdram_dq' display the data from text file depend on the input switch. Below is the example of seven segment from address '02'.

TABLE 3. Example of 7-segments of SDRAM at address '2f'

HEX	Binary	7-segments display
HEX3	1000000	
HEX2	0010010	
HEX1	0000000	
HEX0	1000000	

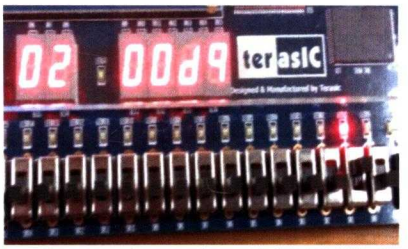

Fig.10 Example output of SDRAM display on FPGA

In the figure 10 is the example of one of the output display from seven segments on FPGA board of SDRAM controller. Input from switch '0010' provide data from text file of the address '02' that contains data '0580'. The following data tabulate in the table below:

TABLE 4. Output data tabulated from SDRAM

Switch	Address(Hex)	Output(Hex)
0000	00	0204
0001	01	0982
0010	02	00D9
0011	03	8F70
0100	04	0A8C
0101	05	03B1
0110	06	02BA
0111	07	06E9
1000	08	0A1D
1001	09	01AB
1010	0A	00AA
1011	0B	0230
1100	0C	0125
1101	0D	018B
1110	0E	0B0C
1111	0F	FFFF

Table above are the result from the of SDRAM controller. All input was simulated on Quartus software and tested on FPGA board. The input switch is same to the address because it represents the sequence of data from text file. The result from both method is true when compare to the data in the text file. This can be assumed the SDRAM controller is work well.

i. FLASH

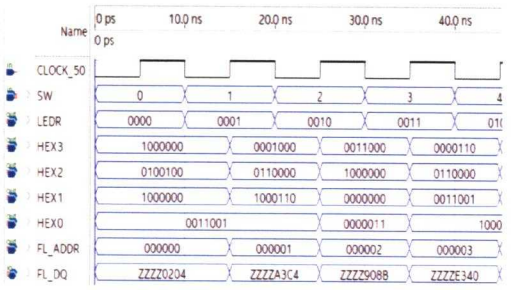

Fig. 11. Waveform of FLASH

Figure above shows the waveform of FLASH memory. 'Fl_addr' count the address from text file while 'fl_dq' display the data from text file depend on the input switch. Below is the example of seven segment from address '00'.

TABLE 5. Example of 7-segments of FLASH at address '00'

HEX	Binary	7-segments display
HEX3	1000000	
HEX2	0010010	
HEX1	0000000	
HEX0	1000000	

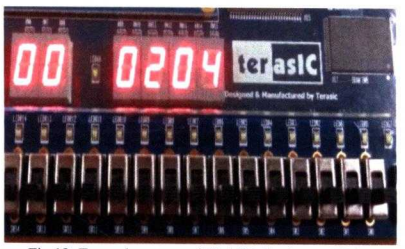

Fig.12. Example output of FLASH display on FPGA

In the figure 12 is the example of one of the output display from seven segments on FPGA board of FLASH controller. Input from switch '0000' provide data from text file of the address '00' that contains data '0204'. The following data tabulate in the table below:

TABLE 7. Output data tabulated from FLASH

Switch	Address(Hex)	Output(Hex)
0000	00	0204
0001	01	A3C4
0010	02	908B
0011	03	E340
0100	04	FE90
0101	05	409A
0110	06	8EAF
0111	07	01EC
1000	08	60A5
1001	09	9183
1010	0A	00FF
1011	0B	023C
1100	0C	1250
1101	0D	018E
1110	0E	00FF
1111	0F	0EFA

Table above are the result from the of FLASH controller. The input switch is same to the address because it represents the sequence of data from text file. All input was simulated on Quartus software and tested on FPGA board. The result from both method is true when compare to the data in the text file. This can be assumed the flash controller is work well.

B. Area

The basic logic unit of the module in FPGA is the configuration of logic block or known as logic cells. This area can be measure using Fitter report. Quartus software calculated the number of half-adaptive logic modules that are available in the device. The fitter report defines combinational ALUT / register pairs used to specify half-adaptive logic modules. It also calculated logic module by estimating how many half adaptive logic modules to fit the design and indicate in a percentage of the total number of half-adaptive logic modules in the FPGA. The logic utilization used is (A-B+C) / (Total number of half-adaptive logic modules in the device).

TABLE 8. Result data of area

Types of Memory	**Area /Total logic elements**
SRAM	88 / 114,480 (<1%)
SDRAM	89 / 114,480 (<1%)
FLASH	83 / 114,480 (<1%)

Table above shows the result of area / total logic element for SRAM, SDRAM, and, FLASH memory controller that obtained from Fitter report in Quartus software. From the observation, flash memory has minimum total logic element that is 83 / 114,480 (< 1%). SDRAM has maximum total logic area that is 89 / 114,480 (<1%) while SRAM has 88 / 114,480 (<1%). Below shows the pie chart of area data from each memory.

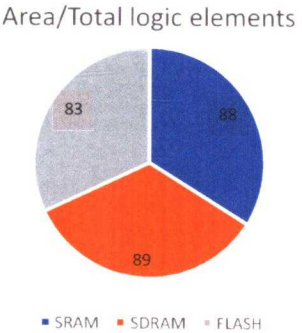

Fig.13 Pie chart of area

C. Power

The power consumption for SRAM, SDRAM and FLASH memory indicated using Powerplay Power Analysis tools that can estimate device power consumption accurately. There are two types of power analysis need to be consider that is Thermal planning and Power supply planning. Thermal power is the heat dissipates from FPGA and Power supply is the power need to run the device. These two Power analysis are related because much of the power supplies from device dissipates as heat.

TABLE 9. Result data of power

Types of Memory	I/O Thermal Power Dissipation	Core Static Thermal Power Dissipation	Total Thermal Power Dissipation
SRAM	77.15mW	98.61mW	175.76mW
SDRAM	71.26mW	98.59mW	169.85mW
FLASH	77.03mW	98.61mW	175.64mW

The table 9 is the result of power consumption for SRAM, SDRAM, and FLASH memory. Total thermal power is summation of input and output thermal power and core static thermal power. Input and output thermal power consumed due to the charging and discharging between from external capacitors and device output pins. The core static thermal power is charging or discharging nodes from internal switching due to the device So, the bigger these two value, the bigger the value of thermal power dissipation. SRAM has higher total thermal power with 175.76mW. The lowest is SDRAM with 169.85mw and FLASH memory is 175.64mW that nearly equal with SRAM thermal power dissipation. Below is the chart to differentiate all type of memory in term of its total thermal power consumption.

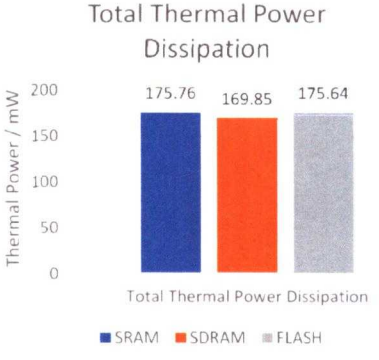

Fig.14. Chart of power

From the research, there are several factors that affect to the power consumption such as device selection, environmental condition, device resource usage, and signal activities. Power characteristics divide in the different device families. The choice of device also affects the ability of the device to dissipate heat. Signal behaviour like toggle rate and static probability also important of approximation the power consumption.

I. CONCLUSION

All the memories studied were successfully obtained its performance in terms of area and power. The functionality of memory controller also proven by using simulation and FPGA board. In addition, latest technology required small area to optimize the size of logic circuit. Therefore, through this study the best area for memory on chip is FLASH memory. For power performance, recent architecture wants to reduce the power consumption to maintain the battery long life, small power usage and minimize thermal power. This can be concluded the lowest thermal power for memory is SDRAM. All the result from this study successfully achieved as expected.

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Muhamad Aiman Bin Muhamad Aznan (2015859524)

Faculty of Electrical Engineering
Universiti Teknologi MARA (UiTM)
Shah Alam, Selangor
aimanaznan15@gmail.com

ABSTRACT

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INTRODUCTION

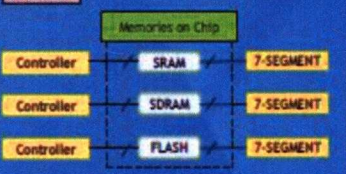
This project is to studies and analyze memories performance on the FPGA board. The performance such as area and power be obtained by designing controller using Verilog code. Result was collected through Quartus software. Inside Quartus itself, it has Timing Analyzer, Power Tools, and Fitter to check the power, and area. The controller also tested on the FPGA board. Specific FGPA board that used is Altera DE2-115 to run this project. The main purpose of this project is to facilitate to future students to make reference. This is because there is lack of study in details about the memory on chip performance and all the information can be used for future student as their reference.

OBJECTIVE

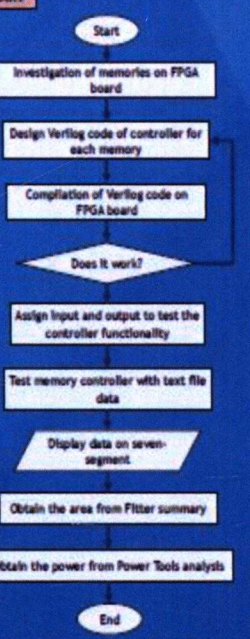
1) To determine the performance for SRAM, SDRAM and FLASH memory on FGPA board in term of its area and power
2) To analyze and compare the area and power for each memory
3) To test and simulate the memory controller on FPGA board and Quartus software

METHODOLOGY

BLOCK DIAGRAM

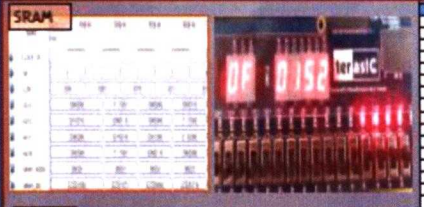


FLOWCHART



RESULTS

SRAM

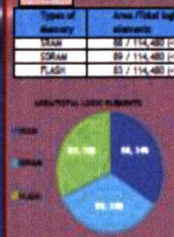


SDRAM

FLASH

AREA

Types of Memory	Area (Total logic elements)
SRAM	88 / 114,480 (<1%)
SDRAM	89 / 114,480 (<1%)
FLASH	83 / 114,480 (<1%)



POWER

Types of Memory	I/O Thermal Power Dissipation	Core Static Thermal Power Dissipation	Total Thermal Power Dissipation
SRAM	77.15mW	98.61mW	175.76mW
SDRAM	77.35mW	98.59mW	175.94mW
FLASH	77.23mW	98.61mW	175.84mW

CONCLUSION

All the memories studied were successfully obtained its performance in terms of area and power. The functionality of memory controller also proven by using simulation and FPGA board. In addition, latest technology required small area to optimize the size of logic circuit. Therefore, through this study the best area for memory on chip is FLASH memory. For power performance, recent architecture wants to reduce the power consumption to maintain the battery long life, small power usage and minimize thermal power. This can be concluded the lowest thermal power for memory is SDRAM. All the result from this study successfully achieved as expected.