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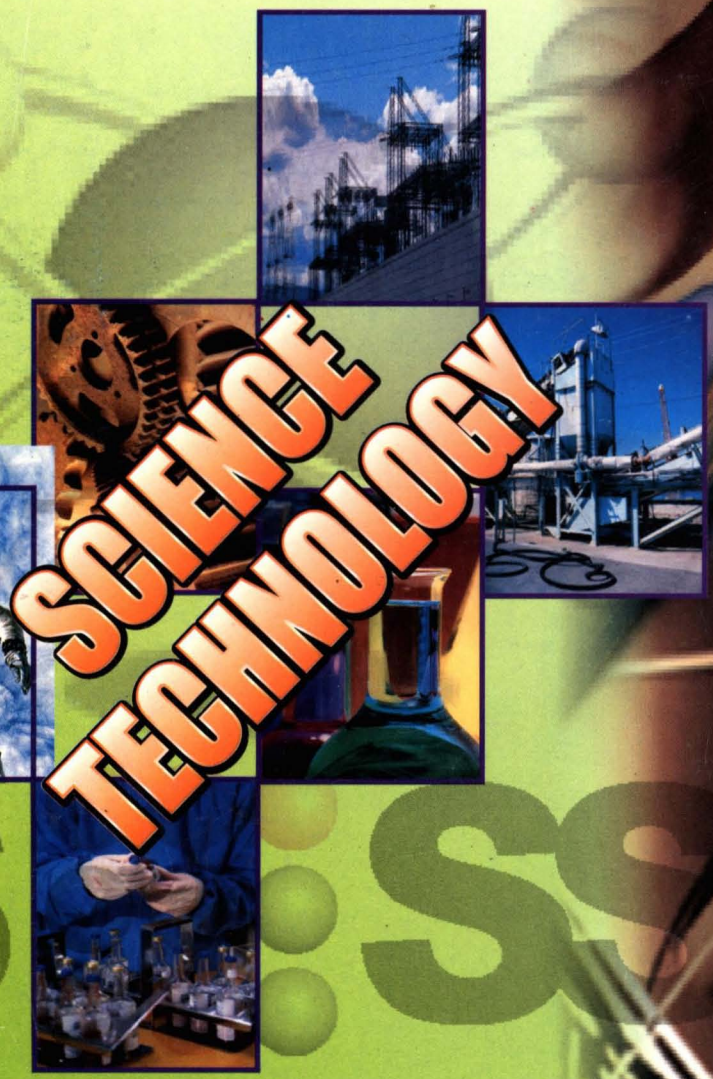

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Evaluating and Implementing Noise Tolerance Precharge in Full Adder

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ABSTRACT

The semiconductor device now day are dealing with the Very Large Scale Integrated (VLSI) circuit for performing the component such as logic, adder, multiplexer and other device. But in order to function in normal condition or in high speed condition the output node of the circuit are influence by the several type of noise in deep submicron circuit. The noise will cause the circuit produce the error output. To overcome this problem, one technique has been used. The technique is Noise Tolerance Precharge circuit design. In this paper the Noise Tolerance Precharge circuit will be combining into the Complementary Metal Oxide Semiconductor (CMOS) circuit. The comparison for each result show the Noise Tolerance Precharge circuit output is more noise-immune and display batter result. The implemented circuits with Noise Tolerance Precharge result show the circuit is reduce noise 90% of the error in normal domino technique. The designs in this paper are based on MOS 0.35μ technology.

Keywords: *Deep submicron, CMOS, Noise tolerant, XOR-XNOR circuits, adder.*

Introduction

The low-voltage CMOS VLSI device is a combination of two type circuit. Dynamic and static circuit is the major circuit combination to produce the VLSI system. The noise-tolerance-precharge (NTP) is the important part in the low-voltage CMOS VLSI system. In high-speed system, the dynamic logic circuit techniques are frequently used (James, B. Kuo et. al. 1997). During operation of the system there are noise or disturbance produce by the logic. Noise sources that have substantial impact on the performance of digital circuits include ground bounce, crosstalk, charge sharing, process variations, charge leakage, alpha particles and electro-magnetic radiation. (Lei Wang et. al. 2000). The noise-tolerance-precharge (NTP) technique is the solution for the problem.

Static Circuit

The XOR and XNOR gates play the major rule in various circuits especially circuits used for performing arithmetic operations like full adders, compressors, comparators, and so on. That circuit proved to be power efficient but they displayed poor delay characteristics. To overcome the problem of skewed output an efficient design that combines the implementation of both the XOR and the XNOR functions in one circuit using only 6 transistors is presented in Figure 1 (Lei Wang et. al. 2000). The circuit has a single connection to Vdd and a single connection to Gnd with no direct connection between them. The existence of Vdd and Gnd connections give good driving capability to the circuit and the elimination of direct connections between them avoids the short circuit currents component. An improved version of this circuit in Figure 2 has a better power delay product and higher noise immunity.

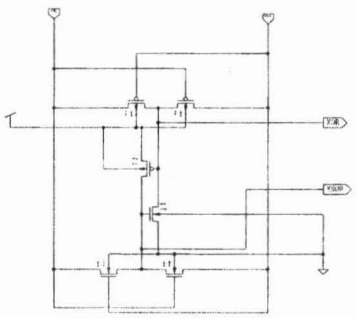


Fig. 1: The Schematic of XOR-XNOR Logic

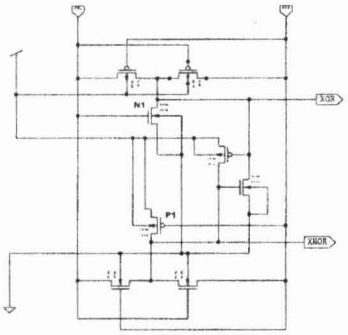


Fig. 2: The Schematic of XOR-XNOR Logic with NTP

Full Adder Circuit

The 1-bit full adder is the basic of the adder circuit. Basically the full adder has three inputs and two outputs. The logic circuit of the one bit full adder is shown in Figure 3.

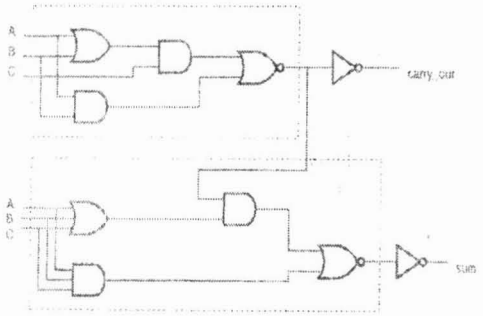


Fig. 3: The One-Bit Static Full Adder (Pucknell, D. et. al. 1985)

A One bit adder work with add the all input and the will shown the result of adding all of input. When fully function the adder will follow the truth table result as bellow.

Refer to figure above the static block diagram are needed while designing in the L-edit software. The block diagram shows the input part (A, B, and C) and output part (Sum and Carry). The Boolean equation of this adder is (Vai, M. M. 2001):

$$SUM = ABC + A\overline{B}\overline{C} + \overline{A}\overline{B}C + \overline{A}B\overline{C} \quad (1)$$

$$CARRY = AB + AC + BC \quad (2)$$

where

A, B, C = input

Dynamic Circuit

While Designing the adder using dynamic technique or domino technique the basic speciation almost same as the designing the adder in static circuit. The Boolean equation and the truth table of dynamic circuit are equal for the static technique. Refer to Figure 4 the circuit bellows show the one-bit dynamic adder.

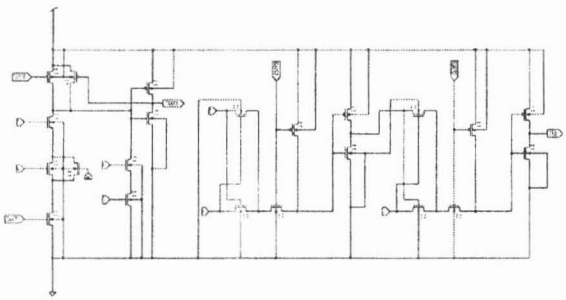


Fig. 4: The Circuit Schematic of Normal One Bit Adder.

Implementation of the Noise Tolerance Precharge (NTP) into circuit has been made in this project. The dynamic NTP technique has been used into the dynamic circuit in Figure 5. The specifications of this circuit are almost same like the normal technique but the circuit has been modified follow the dynamic NTP technique.

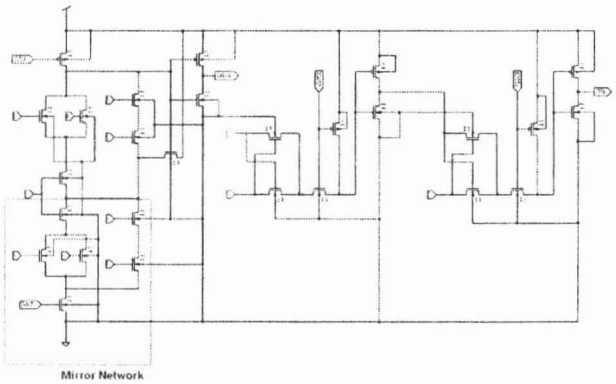
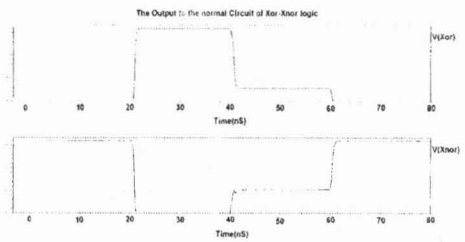


Fig. 5: The Circuit Schematic of One Bit Adder with NTP Technique.

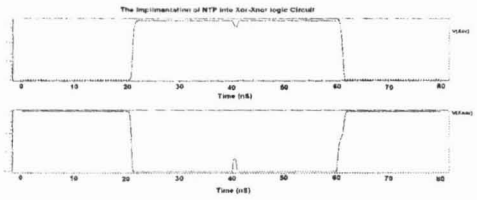
Simulation Result

The result of the circuit is grouping into two categories.

Result of Static Circuit
We will now compare the effectiveness of NTP in reducing the noise precharge which is generated by the static circuit.



(a)

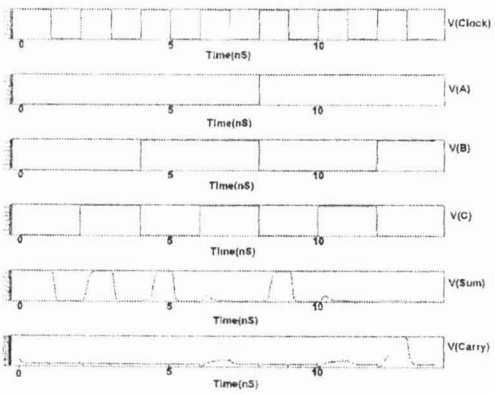


(b)

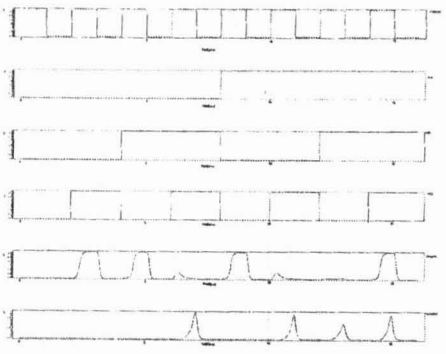
Fig. 7: The Output for XOR-XNOR Circuit (a) without NTP (b) with NTP

The result in Figure 7(a) shows that the XOR-XNOR has error output. It happens at 40ns until 60ns. By adding NTP technique, the result in Figure 7(b) is success. This indicates that the NTP technique is effective in reducing the precharge error.

Result of Dynamic Circuit



(a)



(b)

Fig. 9: The Output for the Adder Circuit (a) without NTP (b) with NTP

Figure 9(a) shows the output of one bit full adder without NTP still has noise prechage. Hence Figure 9(b) shows full adder with NTP. The output is true based on the true table.

Table 1: Truth Table for Full Adder with NTP and without NTP.

No	INPUT				Truth Table		Normal		NTP	
	Clock	A	B	C	SUM	CARRY	SUM	CARRY	SUM	CARRY
1.	↑	0	0	0	0	0	1	0	0	0
2.	↑	0	0	1	1	0	1	0	1	0
3.	↑	0	1	0	1	0	1	0	1	0
4.	↑	0	1	1	0	1	0	0	0	1
5.	↑	1	0	0	1	0	1	0	1	0
6.	↑	1	0	1	0	1	0	0	0	1
7.	↑	1	1	0	0	1	0	1	0	1
8.	↑	1	1	1	1	1	1	1	1	1

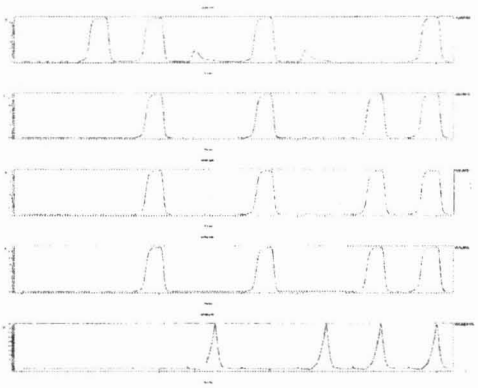


Fig. 10: The Output for the Implementation NTP into Four Bit Adder Circuit.

That Figure 10 shows the output of 4 bit full adder. Based on that simulation output it indicates the NTP technique can make the output is more noise-immune and batter.

Conclusion

Trough this study, the processes analyzed and implementation of NTP circuit into static and dynamic circuit has been successful. Using the 0.35μ MOS technology the NTP has been implemented into XOR-XNOR fast logic for the static section. In the dynamic section the NTP technique has been implemented into one-bit adder and four bit adder. Using the T-spice the circuit has been analyzed using the transient analysis. The circuit has been injected by the input and the output has been produce in W-edit. The output of W-Edit has been used as result and been analyzed. The concept of NTP technique has been prove true with ability of reducing the noise in both type of circuit dynamic and static circuit. The ability of the NTP produces more than 90% effective circuit compare between normal techniques. In other section the NTP also been proved to work normally in high speed of circuit. It has been show in the dynamic section when the circuit has been injected with high speed clock cycle. At the last all the theoretical research at the literature review has been proved by the analysis in section dynamic and static circuit.

References

Andrei, V. (1994). *The Spice Book*. Canada: John Wiley & Sons, Inc.

Baker, R.J., HarryW.Li & David, E. B. (1998). *CMOS Circuit Design, Layout and Simulation*. New York: Wiley Inter Science.

Davari, B., Dennard, R. H. & Shahidi, G. G. (1995). *CMOS Scaling for High Performance and Low Lower—The Next Ten Years*. IEEE Pwc., 83(4): pp. 595-606

Friedman, V. & Liu, S.I.. (1984). Dynamic Logic Circuits. *IEEE J. Sol. St. Ckts.*, Vol. 19: pp. 263 – 266.

James, B. Kuo & Jea-Hong Luo. (1997). *Low Voltage CMOS VLSI circuits*. Taipei,Taiwan: Wiley-Interscience Publication.

John Y Chen. (1990). *CMOS Devices and Technology for VLSI*. Englewood Cliffs.

Kenneth L. Shepard & Virod Narayan. (1996). *Noise in Deep Submicron Digital Design*. Yorktown Height: IBM T.J Research Center.

Ko-Chi Kuo & Brandley S.Carlson. (2001). High Performance Cmos Static Logic Circuit Design. *Proceeding of 44th 2001 IEEE symposium.*

Lei Wang & Naresh Shanbhag (2000). *Noise –Tolerant Dynamic Circuit Design*. IEEE Pwc.

Mohamed, E., Sumeer, G., & Magdy B.Noise. (1993). *Tolerant Low Voltage XOR-XNOR for Fast Arithmetic.* New Jersey: Prentice-Hall.

Pucknell,D.A & Eshraghian,K. (1985). *Basic VLSI Design*. Australia: Prentice-Hall.

Roger, L. T. (1996). *Digital Electronic Principle and Application*. 5th ed. McGraw-Hill: pp. 38-40.

Saburo Muroga. (1982). *VLSI System Design: When and How to Design Very-Large-Scale Integrated Circuit.* Illinois, Urbana: A Wiley-Interscience Publication.

Shimohigashi, K. & Seki, K. (1993). Low-Voltage ULSI Design. *EEE J. Sol. St. Ckts.*, 28(4), 40813.

Sung-Mo Kang & Leblebici, Y. (1998). *CMOS Digital Integrated Circuits Analysis and Design*.2nd ed. Illinois, Urbana: McGraw Hill.

Vai,M.M. (2001). *VLSI Design*. 1st .ed. Boca Raton, Florida:CRC Press LLC.

Yannis, P. T. (1987). *Operation and Modeling of the MOS Transistor*. N.Y.: McGraw Hill.

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