INVESTIGATION OF LATCH-UP BEHAVIOUR IN 0.5 MICRON CMOS TECHNOLOGY

INSTITUT PENYELIDIKAN, PEMBANGUNAN DAN PENGKOMERSILAN
UNIVERSITI TEKNOLOGI MARA
40450 SHAH ALAM, SELANGOR
MALAYSIA

BY :

WAN FAZLIDA HANIM
SUHANA SULAIMAN
MOHD JAMIL NAPIAH

JUNE 2005

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Biro Penyelidikan dan Perundingan
Universiti Teknologi MARA
40450 Shah Alam, Malaysia
Tel : 03-55442094 / 5 / 3 / 2 Fax : 03-55442096
Website : www.uitm.edu.my/brc

UNIVERSITI TEKNOLOGI MARA

Penolong Naib Canselor
(Penyelidikan)
03-5544 2094/5
aznizl32@salam.itm.edu.my

Koordinator Penyelidikan
(Sains dan Teknologi)
03-5544 2091
#mansur 628@salam.uitm.edu.my

Koordinator Penyelidikan
(Sains Kemasyarakatan &
Kemanusiaan)
03-5544 2097
rosmimah@salam.itm.edu.my

Koordinator Perundingan
(Kewangan)
03-5544 2090
shidah@salam.itm.edu.my

Koordinator Perundingan
03-5544 2100
aro@salam.itm.edu.my

Penolong Pendaftar
03-5544 2092
intan 553@salam.itm.edu.my

Pegawai Eksekutif
03-5544 2098
rohani734@salam.itm.edu.my

Pentadbiran
03-5544 2093

Unit Kewangan Zon 17
03-5544 2099
03-5544 3440
03-5544 2089
453mohdh@salam.itm.edu.my

Surat Kami : 600-BRC/ST.5/3/576
Tarikh : 30 Jun 2003

Puan Wan Fazlida Hanim Abdullah
Fakulti Kejuruteraan Elektrik
Universiti Teknologi MARA
40450 Shah Alam

Puan

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Dengan hormatnya perkara di atas adalah dirujuk.

Sukacita dimaklumkan bahawa Mesyuarat Jawatankuasa Penyelidikan ke-67 pada 30 Jun 2003 telah membuat keputusan:

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ii. Tempoh projek penyelidikan ini ialah **12 bulan**, iaitu bermula **1 Julai 2003** hingga **30 Jun 2004**.

iii. Kos yang diluluskan ialah sebanyak **RM 20,000.00** sahaja. Penggunaan geran yang diluluskan hanya akan diproses setelah perjanjian ditandatangani.

iv. Semua pembelian peralatan yang kosnya melebihi RM 500.00 satu item perlu menggunakan Pesanan Jabatan Universiti Teknologi MARA (LO). Pihak puan juga dikehendaki mematuhi peraturan penerimaan peralatan. Panduan penerimaan peralatan baru dan pengurusannya, dilampirkan.

v. Semua peralatan/kelengkapan penyelidikan yang dibeli adalah menjadi hak milik fakulti. Semua peralatan/kelengkapan hendaklah diserahkan kepada pihak fakulti setelah tamat penyelidikan untuk kegunaan bersama.

vi. Seperti yang puan sedia maklum puan perlu membentangkan kertas kerja di Seminar Hasil Penyelidikan BRC setelah projek tamat dijalankan nanti.

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vii. Kertaskerja boleh dibentangkan di seminar selain daripada yang dianjurkan oleh BRC setelah 75% deraf awal laporan akhir projek dihantar ke Biro untuk semakan. Walaubagaimanapun, puan perlu membuat permohonan kepada Biro penyelidikan dan Perundingan.

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ix. Puan perlu menandatangani Borang Perjanjian Penyelidikan (disertakan) dan menyerahkannya kembali kepada pihak Biro dengan kadar segera.

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Yang benar,

PROF. DR AZNI ZAIN AHMED
Penolong Naib Canselor (Penyelidikan)

s.k.

1. Timbalan Naib Canselor (Pembangunan dan Penyelidikan)
   Universiti Teknologi MARA

2. Dekan
   Fakulti Kejuruteraan Elektrik

3. Penolong Akauntan
   Unit Kewangan Zon 17
   Biro Penyelidikan dan Perundingan

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Tarikh : 22 Jun 2005
No. Fail Projek : 600-BRC/ST.5/3/576

Penolong Naib Canselor (Penyelidikan)
Institut Penyelidikan, Pembangunan dan Pengkomersilan
Universiti Teknologi MARA
40450 Shah Alam

Ybhg. Prof.,

LAPORAN AKHIR PENYELIDIKAN "INVESTIGATION OF LATCHUP BEHAVIOUR IN 0.5 μM CMOS TECHNOLOGY"

Merujuk kepada perkara di atas, bersama-sama ini disertakan 3 (tiga) naskah Laporan Akhir Penyelidikan bertajuk "Investigation Of Latchup Behaviour In 0.5 μM Cmos Technology".

Sekian, terima kasih.

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WAN FAZLIDA HANIM
Ketua
Projek Penyelidikan

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PROJECT TEAM MEMBERS

WAN FAZLIDA HANIM
Project Leader

....
Tandatangan

SUHANA SULAIMAN
Project Member

....
Tandatangan

MOHD JAMIL NAPIAH
Project Member

....
Tandatangan

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PENGHARGAAN

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TABLE OF CONTENTS

1.	Introduction	
1.1	Latch-up in CMOS ICs	1
1.2	Research Objectives	2
1.3	Scope of Work	2
1.4	Structure of Report	3
2.	Theory: Latch-up in CMOS Technology	
2.1	Parasitic Bipolar Junction Transistor	4
2.2	Triggering Mechanisms	5
2.3	Latch-up Models	6
2.4	Handling Latch-up	8
3.	Material & Methodology	
3.1	Device Fabrication	9
3.2	Equipment Setup	13
3.3	Measurement Approach	14
4.	Research Findings: Test Structures and Measurement Setup	
4.1	Test Structure Description	16
4.2	Measurement Setup on Test Structure	17
4.3	Algorithm Flowchart	18
4.4	Program Listing	19
4.5	Software Validation	20
4.6	Conclusion	22
5.	Results and Discussion	
5.1	SCR Characteristics of 0.5 micron CMOS Structure	23
5.2	Investigation on n+ to p+ Separation	24
5.3	Conclusion	27
6.	Conclusion	
6.1	Conclusion on Measurement Approach	28
6.2	Conclusion on Latch-up Performance	28
6.3	Further Works	29

References 30
Appendix A: Fabrication Details
Appendix B: Measurement Algorithm for Software Validation
Appendix C: Simulation Input Files

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LIST OF FIGURES

Figure		
2.1	Cross-section of bulk silicon CMOS inverter showing vertical PNP and lateral NPN parasitic bipolar transistor forming a feedback loop	4
2.2	IV curve for NMOS exhibiting latch-up behaviour under gate bias with different regions of operation	6
2.3	(a) Cross-section of an NMOS transistor showing the currents in the parasitic NPN transistor. (b) Cross-section of an NMOS transistor showing the parasitic NPN transistor and a topside substrate contact	7
2.4	Substrate resistance model due to multiple current sources	7
2.5	Substrate resistance models due to multiple substrate contacts	8
3.1	N-channel device structure from 0.5 micron technology used as samples for latch-up characterization	12
3.2	Block diagram of device characterization system	14
3.3	For parametric extraction, all sites are chosen. For further characterization, only 5 selected sites are chosen.	15
4.1	Summary of latch-up test structure layout and physical cross-section of subchip MDR-2	16
4.2	The parasitic bipolar currents and its equivalent CMOS currents	17
4.3	Measurement setup showing biasing plan	18
4.4	Programming algorithm to obtain the required data I_{total} vs. V_{p+}	19
4.5	Parametric data measurement verification of 0.6 μm gate-length performance	21
4.6	Sweep data measurement verification of Agilent 4073 setup	21
5.1	Measured characteristics of SOI and bulk pnpn of 2/2 μm distance between n+/p+ to well edge	23
5.2	N-well current investigation on SOI and bulk device of 2/2 μm n+/p+ to well edge distance	25
5.3	Trigger current vs. n+ to p+ separation for SOI and bulk devices	26
5.4	Holding voltage vs. n+ to p+ separation for SOI and bulk devices	27

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LIST OF TABLES

Table		
3.1	Fabrication method in chronological order of 0.5 µm NMOS and PMOS on SOI substrate fabrication process based on the preparation of lot X126 runcard	10
3.2	Lot pan showing 6 splits with 2 wafers assigned to each group	15
5.1	Trigger and holding conditions of latchup characteristics presented in Figure 5.1	24

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LIST OF ABBREVIATION

BESOI	Bond-and-Etch-Back Silicon-On-Insulator
BJT	Bipolar Junction Transistor
BSOI	Bonded Silicon-On-Insulator
CMOS	Complementary Metal-Oxide-Semiconductor
DIBL	Drain-Induced Barrier Lowering
FDSOI	Fully-Depleted SOI
g_D	Drain Conductance
g_m	Gate transconductance
I_{DS}	Drain Current
I_{p+}	current from PMOS source/diffusion region
L_g	gate length
LNPN	Lateral NPN bipolar transistor
MIMOS	Malaysian Institute of Microelectonics System
MOSFET	Metal-Oxide-Semicondcutor Field-Effect-Transistor
NMOS	n-channel MOSFET
PDSOI	Partially-Depleted SOI
PMOS	p-channel MOSFET
r_D	Drain resistance
SIMOX	Separation by Implantation of Oxygen
SOI	Silicon-On-Insulator
VDS	Drain-to-Source Voltage
VFB	Flat-band Voltage
V_{p+}	voltage at PMOS source/drain diffusion region
VPNP	Vertical PNP bipolar transistor

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Abstract

The research project investigates available latch-up test structures from MIMOS Berhad and covers current-voltage characterization of silicon-controlled rectifier behaviour of parasitic BJTs in CMOS technology. Measurement setup utilizing the structures for IV measurements are designed. A suitable measurement routine for the testing of latch-up in MOS device engineering at wafer level is developed for use in research environment. Tests are done on available MIMOS test structures representing twin tub technology and silicon-on-insulator substrate using automatic semiconductor characterization system comprising of Semiconductor Parametric Characterization Software (SPECS), UFK200 automatic prober and Agilent 4073 tester. Avalanche induced latch-up of three types of device were demonstrated: SOI without thickness adjustment, SOI with thinner layer due to thickness adjustment and bulk silicon control device are demonstrated. Immunity towards latch-up is improved for devices on BSOI substrate.

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Chapter 1:
Introduction

1.1 Latch-up in CMOS ICs

Latch-up is the behaviour of Metal-Oxide-Semiconductor Field-Effect-Transistor (MOSFET) when parasitic Bipolar Junction Transistors (BJT) inherent in its structure turns on. The resultant current flowing can eventually lead to overheating, if not controlled. Integrated circuits (ICs) are often destroyed by overheating commonly attributed to the latch-up phenomenon.

Failure Analysis (FA) techniques are used after IC packaging to investigate cases of overheating in ICs and assumes that overheating may be the effect of latch-up. However, this does not explain the parasitic BJT behaviour nor does it allow any form of prediction of the susceptibility of the device technology against latch-up.

In MIMOS Berhad, test structures are obtained as part of previous technology transfer from Japan and Germany. However, the documentation on latch-up test structures are not detailed out and described to the basic level of understanding. This issue of device reliability and the source of overheating are often not described. The lacking of such understanding would eventually result in the local industry ignoring the possibility of latch-up that is detrimental to the circuit reliability.

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1.2 Research Objectives

The motivation for the research work is to characterize the current-voltage behaviour of silicon-controlled rectifier behaviour of parasitic BJTs in CMOS technology. The research work aims to study the available latch-up test structures in industrial practice and suggest ways to utilize the structures. From a detailed understanding of the test structures, the work aims to develop a suitable measurement routine for the testing of latch-up in MOS device engineering at wafer level for use in industrial research environment. Applying the measurement setup established, the work compares latch-up behaviour of CMOS technology on bulk silicon substrates to SOI wafers.

1.3 Scope of Work

The laboratory work is carried out in MIMOS Berhad. The work focuses latch-up characterization using automatic semiconductor characterization system comprising of Semiconductor Parametric Characterization Software (SPECS), UFK200 automatic prober and Agilent 4073 tester.

Tests are done on available MIMOS test structures representing twin tub technology and silicon-on-insulator substrate. Samples are taken from lot X126; wafer #2 to reflect CMOS technology on SOI substrate with mean thickness 1.5 um, wafer #9 to reflect SOI wafer with mean thickness 0.7 um and wafer #18 for bulk silicon CMOS technology.

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1.4 Structure of Report

The theoretical background of parasitic BJT behaviour leading to latch-up is covered in chapter 2. Chapter 3 presents the material preparation and the available resources and infrastructure utilized in the project. These include the device fabrication of the samples and the equipment setup. Chapter 4 details out the findings of investigation on available test structures and the measurement algorithm developed to generate the necessary data using HPBASIC. Chapter 5 then compares latch-up beahviour of 0.5 micron bulk CMOS technology and 0.5 micron CMOS technology on SOI substrate.

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Chapter 2:
Theory: Latch-up in CMOS Technology

2.1 Parasitic Bipolar Junction Transistors

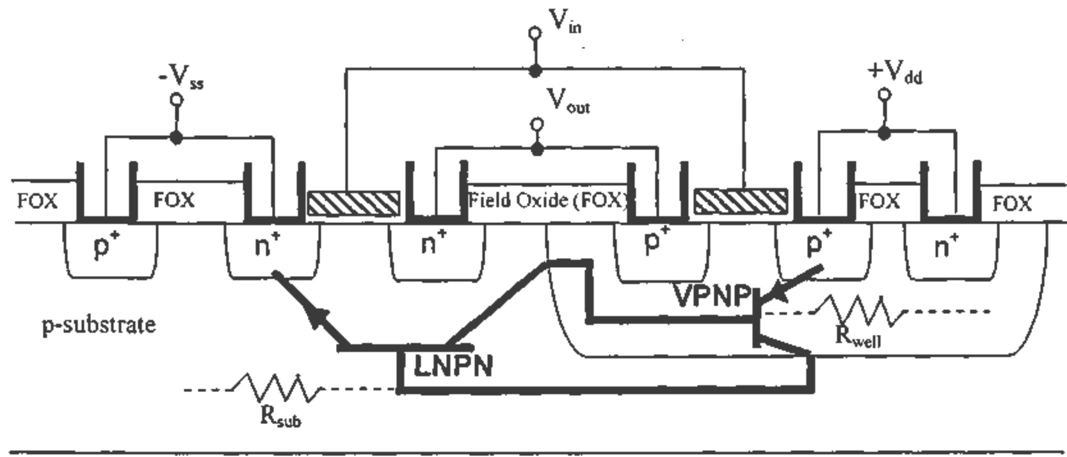

Figure 2.1: Cross-section of bulk silicon CMOS inverter showing vertical PNP and lateral NPN parasitic bipolar transistor forming a feedback loop [1].

Inherent in the CMOS structure are two types of parasitic bipolar transistors - vertical PNP (VPNP) and lateral NPN (LNPN) bipolar transistors. VPNP is formed by the p+ source as emitter, the n-well as base and the p-type substrate as collector; LNPN by the n+ drain as emitter, p-type substrate as base and the n-well as the collector as shown in Figure 2.1.

As the CMOS are scaled down, the distance between the n+/p+ source/drain diffusion distances to the edge of the well is reduced. The closer the distance, the better the performance of unwanted bipolar transistors. The closer distance leads to a thinner base. Since the collector of each Bipolar Junction Transistor (BJT) drives the base of the other, a feedback loop is formed with a loop gain $\beta_{NPN}\beta_{PNP}$. The transistors are turned on if the

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base-emitter junctions of the parasitic BJTs are forward biased, possibly due to transient or lateral currents in the substrate. If the loop gain is greater than 1 and a positive feedback is established, the silicon controlled rectifier like connection results in the device to be in low-impedance high-current state known as latchup [2].

2.2 Triggering Mechanisms

One possible event that can trigger the latch-up behaviour is supply voltages exceeding the absolute maximum ratings. Ratings in data sheets are indication of maximum voltages that can safely be applied. Anything in excess or even close to the conditions may result in breakdown of an internal junction and hence damage to the device or degrade long-term reliability. Ratings should be observed even during both on and off as the triggering mode could result from transients on supply rails.

Input/output pin voltage exceeding either supply rail by more than a diode drop is another possible event triggering latch-up. This could occur as a result of a fault on a channel or input. When part of a system is powered on prior to the supplies being present at a CMOS switch, for example, the powered part of the circuit would be sending signals to other devices in the design which may not be able to handle the voltage levels presented. The resulting voltage levels could exceed the maximum rating of the device, and possibly result in latch-up. Again, this could occur as a result of spikes or glitches on input or output channels.

Another possible event that could lead to latch-up is poorly managed multiple power supplies. CMOS switches that have multiple power supplies tend to be more susceptible to latch-up resulting from improper power-supply sequencing. Such switches usually have two analog supplies, V_{DD} and V_{SS}, and a digital supply, V_L. In some cases, when the digital supply is applied

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prior to the other supplies, it may be possible for maximum ratings to be exceeded and the device to enter a latch-up state.

2.3 Latchup Models

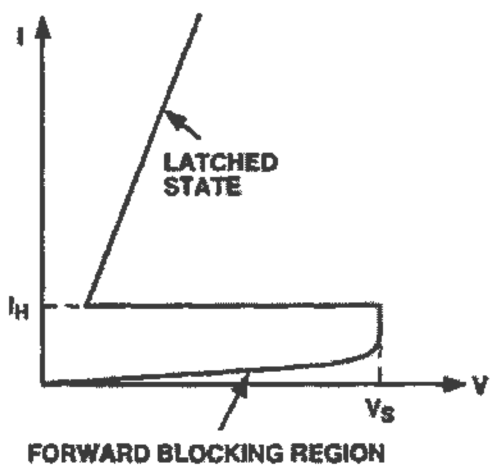

Figure 2.2: IV curve for NMOS exhibiting latch-up behaviour under gate bias with different regions of operation

The generic IV curve for NMOS exhibiting latch-up behaviour under gate bias with different regions of operation is shown in Figure 2.2. The linear and saturation regions governed by standard MOS equations. Region 3 is the bipolar or snapback region. The NMOS transistor operates in the linear and saturation regions under normal conditions. However, it goes into high current regions, namely avalanche breakdown and snapback, during ESD and latchup events. The avalanche generation of carriers in the high-field region near the drain results in the hole current Isub being injected into the substrate. Isub increases the voltage drop across Rsub and raises the local substrate potential Vb, and eventually causes the source-substrate junction to become forward-biased [3].

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Several models have been long reported such as the high-current device models shown in Figure 2.3(a) and (b), substrate resistance network model with external current injection shown in Figure 2.4 and 2.5 for multiple substrate current sources and multiple substrate contacts respectively.

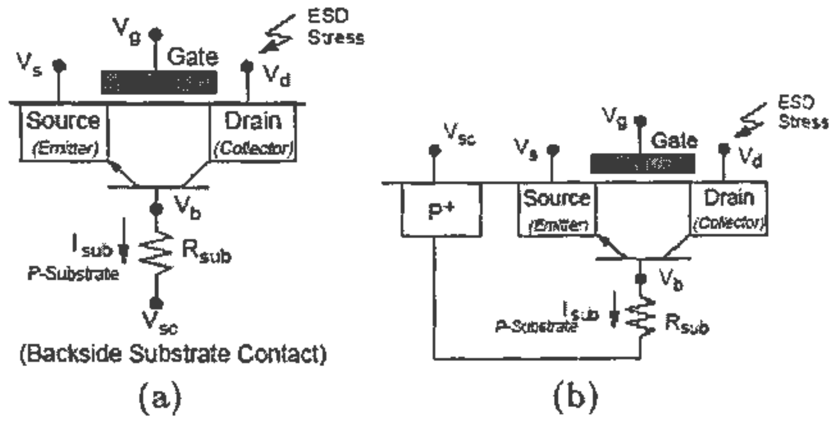

Figure 2.3: (a) Cross-section of an NMOS transistor showing the currents in the parasitic NPN transistor. (b) Cross-section of an NMOS transistor showing the parasitic NPN transistor and a topside substrate contact [4]

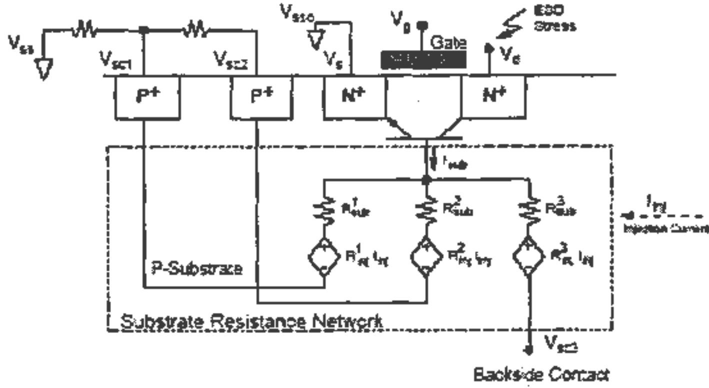

Figure 2.4: Substrate resistance model due to multiple current sources [5]

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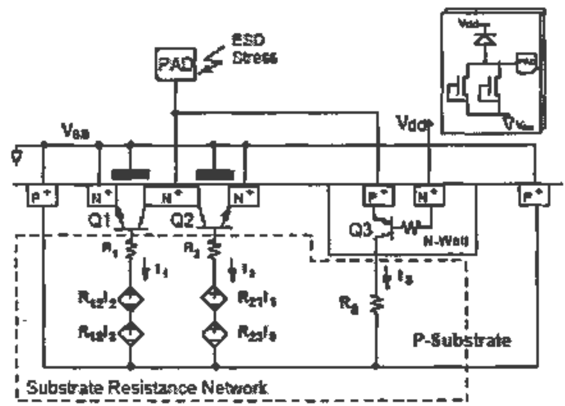

Figure 2.5: Substrate resistance models due to multiple substrate contacts [6]

2.4 Handling Latchup

In bulk silicon, latchup effects are minimized by a retrogade well, a p⁻ epitaxial layer for an n-well process [6] or a twin-tub process instead of an n-well. In SOI, it is possible to totally eliminate CMOS latchup. The excellent isolation that the Buried Oxide provides kill vertical PNP and lateral NPN bipolar transistors between PMOS and NMOS that otherwise would have instigated Silicon-Controlled Rectifier action leading to latch-up. Protection diodes could also be applied in CMOS switches.

If space and cost is a viable option, addition of a diode in series with Vdd could prevent base current from flowing. For cases with multiple supplies, Schottky diodes between the supplies will adequately prevent SCR behaviour and subsequent latch-up.

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Chapter 3:
Material & Methodology

3.1 Device Fabrication

The sample devices used to measure the latch-up characteristics are CMOS structures on bulk silicon substrates as well as bonded silicon-on-insulator (SOI) substrates. The flow of fabrication in chronological order of 0.5 μm NMOS and PMOS on SOI substrate fabrication process based on the preparation of lot X126 runcard is shown in Table 3.1. The table groups the process steps into a list of main steps in chronological order, along with the targeted cross-sections and the relevant descriptions concluded fro the preliminary investigations.

To verify the physical cross-section of the actual fabricated product, scanning electron microscopy (SEM) will be employed to wafer top view for critical dimension monitoring and to a selected wafer cleaved for the purpose. SEM is a type of electron microscope, which is similar to light microscopy, with the exception that electrons are used instead of photons. SEM allows much larger magnifications and better resolution since electron wavelengths are much smaller compared to photon wavelengths [i]. The picture of the n-channel MOSFET SOI device taken by Scanning Electron Microscopy is shown in Figure 3.1. The bulk silicon device is similar to the structure shown except for the presence of the buried oxide.

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Table 3.1: Fabrication method in chronological order of 0.5 μm NMOS and PMOS on SOI substrate fabrication process based on the preparation of lot X126 runcard [ii], [iii], [iv].

STEP 1: WAFER PREPARATION		
a. Wafer coding – to label the wafers		Device layer Buried Oxide Handle Layer
b. 720 nm sacrificial oxidation – to adjust silicon		
c. 2nd marking	Mask alignment	
STEP 2: WELL FORMATION		
a. Well oxidation		Device layer p-well n-well
b. N-well formation: Patterning; Phosphorus Implantation – to form well for PMOS		
c. P-well formation: Patterning; Boron Implantation – to form well for NMOS		
d. Anneal – to activate dopants and remove damage		
e. Drive-In - to achieve specified well depth		
STEP 3: ACTIVE AREA FORMATION		
a. Pad Oxidation – to releases stress on surface due to Nitride		Resist PSG Nitride Pad Oxide
b. Nitride Deposition - to inhibit oxidation during LOCOS formation over the active area.		
c. PSG Deposition - as mask to field-stop implantation and to achieve adhesion with resist		
d. Patterning of Active Area		
STEP 4: LOCOS FORMATION		
a. Field-stop: Boron Ion Implantation – to ensure isolation and reduce series resistance below LOCOS		Field-Stop
b. LOCOS Oxidation: 700 nm - for isolation		
c. Sacrificial Oxidation: 30 nm - to remove nitride thin film		

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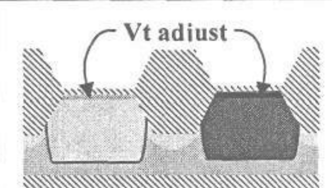
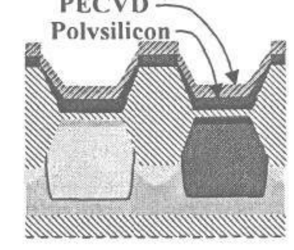
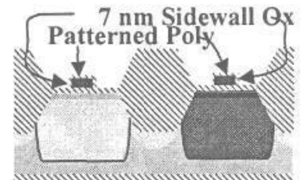
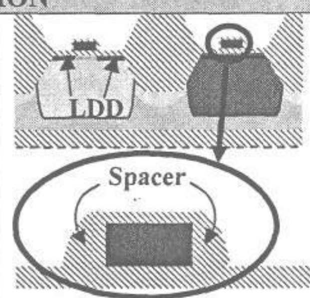
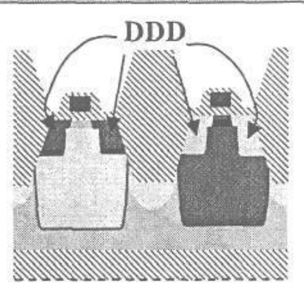
STEP 5: GATE FORMATION	
a. Gate Oxidation: 11 nm - as gate oxide	
b. NMOS Vt adjust: Boron Ion Implantation – to adjusting Vt to desired 0.75 V. No mask. Lower dose ∴ no effect to PMOS.	
c. PMOS Vt adjust: Pattern; Boron Ion Implantation – to make it a buried-channel compensated device. Otherwise Vt too negative compared to NMOS.	
d. Anneal - to activate channel dopant atoms	
STEP 6: GATE ELECTRODE FORMATION	
a. Polysilicon deposition: 300 nm; Implant with Phosphorus; back side etching – to prepare the n+ polysilicon gate electrode	
b. PECVD deposition:160 nm - as a mask during poly ECR etch. Provides better pattern transfer to poly rather than a thick mask.	
c. Gate Electrode Formation: Patterning; PECVD etch; Gate Electrode ECR etch – to form n+ poly gate electrode	
d. Sidewall Oxidation: 7 nm - to replace SiO_2 gate edges that might have been affected by polysilicon ECR etch	
STEP 7: LDD & SPACER FORMATION	
a. N-LDD Formation: Patterning; Phosphorus Ion Implantation; Anneal - to improve reliability, reduce substrate current (esp. critical for NMOS) and improve breakdown voltage.	
b. Spacer Oxide Formation: 16 nm Oxide Deposition; Etch; Anneal – to act as mask to NMOS & PMOS source/drain diffusion implants.	
STEP 8: SOURCE/DRAIN FORMATION	
a. NMOS n^+ diff region formation: Pattern; Arsenic Ion Implantation; Phosphorus Ion Implantation; Anneal - to form graded junctions (Phosphorus diffuses faster than Arsenic) and to reduce hot carrier effects.	
b. PMOS p^+ diff region formation: Pattern; Higher dose of Boron Ion Implantation at lesser tilt angle; Lower dose of Boron Ion Implantation at greater tilt angle - will form a p^- ring around the p^+ regions to reduce hot carrier effects.	
END OF DEVICE PROCESS – PROCEED TO METALLIZATION	

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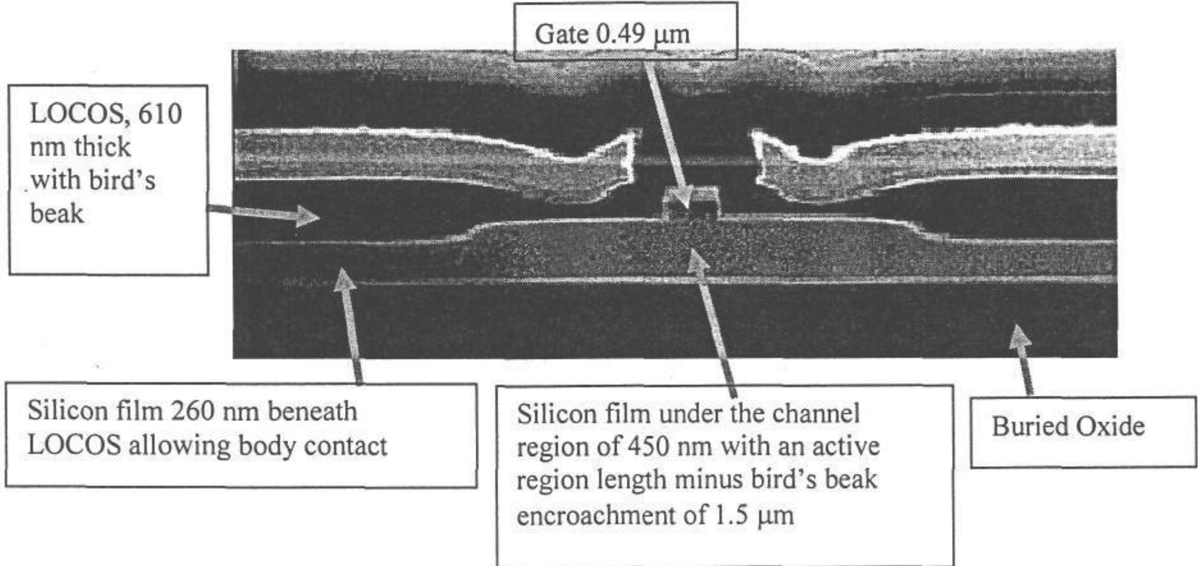

Figure 3.1: N-channel device structure from 0.5 micron technology used as samples for latch-up characterization

SOI device fabrication is aimed to be compatible to the MIMOS 0.5 μm CMOS technology. The reason behind the choice of technology is to strike a balance between available technologies in MIMOS that have been sufficiently investigated and short channel devices to identify SOI characteristics alien to bulk and allow demonstration of SOI substrate to short-channel effects. The type of SOI device to be fabricated suitable with the bonded SOI substrate physical thickness is Partially-Depleted Enhancement-type Inversion-Mode 0.5 μm gate length SOI PMOS and NMOS.

SOI layout is kept fully compatible with the existing masks available to minimize increase in cost incurred. Decision was made on the MIMOS mask product label P018 since it provides sufficient test structures for first round device behaviour investigation

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