ESTEEM Academic Journal
Vol. 19, March 2023, 28-42

The Effect of Gate Geometric Effect and Polysilicon Doping on the Performance of Scaled NMOS

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ARTICLE HISTORY

Received
20 January 2023

Accepted
3 March 2023

Available online
31 March 2023

ABSTRACT

Insufficiently high doping in polysilicon gates of metal oxide semiconductor field effect transistor (MOSFET) becomes unavoidable due to the demands for low-energy ion implantation and limited annealing conditions to achieve ultra-shallow source and drain junctions. This results in the poly-depletion effect for ultra-thin MOSFET, loss of current drive and shift in the threshold voltage. This problem gets intense when the device is further scaled down for the gate length and thickness of gate oxide. Hence, our current work focuses on the effect of gate geometrical effect and polysilicon gate doping on scaled n-channel MOSFET(NMOS) performance. The NMOS device was constructed using TCAD ATLAS tools from SILVACO software. Six different gate lengths of 0.6 μm, 0.4 μm, 0.2 μm, 60 nm, 40 nm and 20 nm were set, and the n-type doping concentration in the polysilicon gate was varied to 1×10^{18}, 1×10^{20} *and* 1×10^{21} cm^{-3} *respectively to see their effect on the NMOS I-V and C-V performances. The findings showed that as the gate length is scaled down, the drain current increases, and as the concentration of the polysilicon doping increases, the value of the threshold voltage, VTH decreases. Based on the simulation and data collected, it can be concluded that the optimum concentration of polysilicon doping that can reduce the poly-depletion effect is* 1×10^{21} $cm^{-3,}$ *and the optimum gate length that can be used to overcome the problem is 20 nm.*

Keywords: *Scaled NMOS, SILVACO TCAD tools, Gate Geometric Effect, Polysilicon Doping*

1. INTRODUCTION

The metal oxide semiconductor field effect transistor (MOSFET) is a semiconductor device widely used for switching purposes and amplifying electronic signals in electronic devices. The introduction of the MOSFET device has brought a change in the domain of switching in electronics. The MOSFET has become the basic building block of very-large-scale integrated (VLSI) circuits, therefore serving as the most important microelectronic device [1]. The MOSFET advantages over other types of devices are its mature fabrication technology, successful scaling characteristics and the combination of complementary MOSFET-yielding CMOS circuits [2]. In MOSFET, a voltage on the oxide-insulated gate electrode can induce a

p-ISSN 1675-7939; e-ISSN 2289-4934

conducting channel between the two other contacts called source and drain. The channel can be n-type or p-type, commonly known as NMOS and PMOS.

In the early days of MOSFET fabrication development, aluminium contact was used as a material for the gate terminal. However, there is a problem ,with using metal as gate contact when the fabrication process involves very high temperature, which will induce an aluminium spike problem [3]. Hence, the use of polysilicon as gate material is introduced. Undoped polysilicon generally has very high resistivity, approximately 108 Ω cm^{-1}. Thus, the polysilicon gate needs to be doped to reduce the resistance. However, in modern CMOS processes, insufficiently high doping in polysilicon gates becomes unavoidable due to the conflicting demands for low-energy ion implantation and limited annealing conditions to achieve ultra-shallow source and drain junctions [4]. This results in poly-depletion effects for ultra-thin oxide MOSFETs, degradation of inversion gate capacitance and transconductance, loss of current drive and a shift in the threshold voltage of the n-MOSFET. This problem gets intense when the device is further scaled down either for the gate length or the thickness of the oxide.

Hence, in this work, scaled NMOS was carried outscaled NMOS was fabricated using SILVACO TCAD to study the poly depletion effectsof ultra-thin oxide on the performance of the NMOS. The optimum polysilicon doping and gate length will be deduced upon the investigation to obtain acceptable gate capacitance and higher transconductance indicating a higher current drive and more stable threshold voltage.

1.1 Polysilicon Doping

In the fabrication of MOSFET, two types of gate material are always used: aluminium metal and polysilicon. Since the semiconductor industry has progressed rapidly over the years, polysilicon was preferred over metal as the gate build material [5]. It is because the conductivity of the polysilicon layer is very low and produces low charge accumulation due to the low conductivity. Thus, a polysilicon layer is doped with n-type or p-type impurities to make it behave as a perfect conductor, which might reduce the delay. For the NMOS device, polysilicon doping is n-type, while p-type impurity is used for the PMOS device.

The concentration of polysilicon doping also plays an essential part in affecting the electrical characteristics of the MOS device [6]. One of the methods that can determine the effect of different concentrations is by using the measurement of flat-band voltage. The flat-band voltage is expressed in equation (1) [7];

$$V_{fb} = \varphi_{ms} - \frac{Q_{ox}}{C_{ox}} \quad (1)$$

The Fermi level is near the conduction band voltage edge for highly doped polysilicon. When the polysilicon is doped moderately, the Fermi level can no longer be assumed to lie near the conduction band edge. As the polysilicon doping is reduced, the gate gets depleted near the polysilicon-oxide interface, and a part of the gate voltage drops across the depletion region of the polysilicon.

p-ISSN 1675-7939; e-ISSN 2289-4934

It has been found that due to the low doping in the polysilicon gate, MOS C-V characteristics degrade [8]. The degradation of MOS capacitance is attributed to the depletion of capacitance in the polysilicon gate. Besides, it was reported that as the polysilicon gate concentration decreases, the degradation in the I-V characteristics becomes more apparent [8].

1.2 Scaling of MOSFET and Gate Geometric Effect

In 1965, a famous law known as Moore's Law was introduced by Gorden Moore. He observed and predicted that the number of transistors per chip in an Integrated Circuit (IC) ouldincrease to two times about every two years. Moore's Law also explained further details about the advancement and rise of growth in transistor technologies, especially in IC design. For the last 40 years, the application growth of the sector has adopted Moore's Law amazingly [9]. When developed in 1960, the channel length of the MOSFET was around 10 μm. Today, most integrated circuits utilise CMOS technology with channel length around 40 nm [10]. The trend of MOSFET gate scaling is shown in Figure 1.

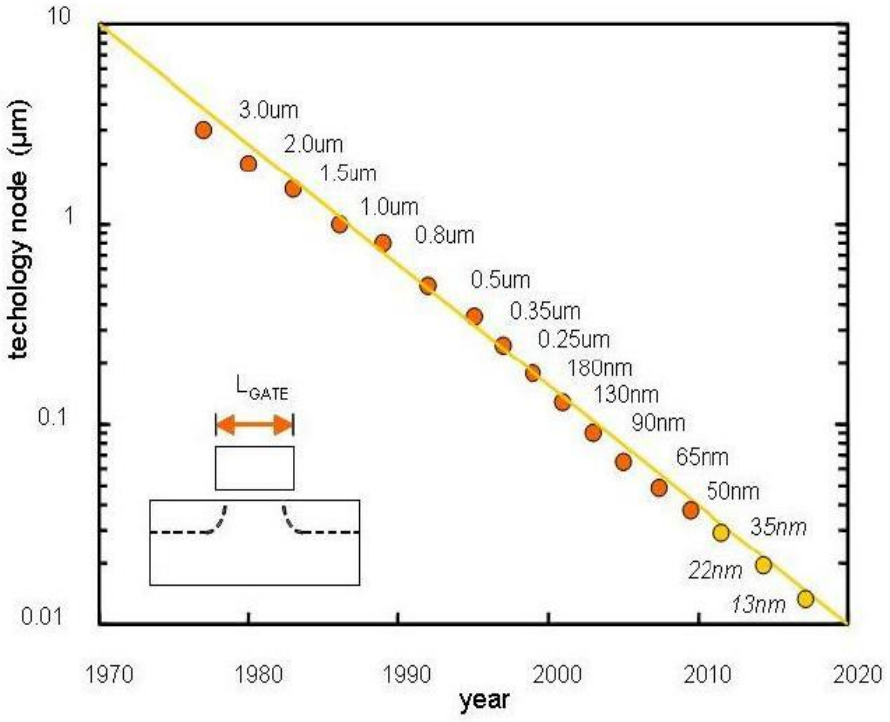

Figure 1: The trend of MOSFET gate length scaling [11].

The scaling projection of MOSFET is required in high-performance applications to achieve the overall chip requirements in terms of speed, power dissipation and efficiency [12]. Many advantages can be obtained by the scaling of MOSFET including the increasing switching speed, the reduction of chip size and the reduction of power dissipation. However, critical challengesinvolved in the scaling projection, such as gate leakage current, polysilicon gate depletion and short channel effects. Thus, th-is work aims to find an optimum gate length that can be used in high-power applications and can avoid those problems.

p-ISSN 1675-7939; e-ISSN 2289-4934

Nowadays, in the development of the semiconductor industry, the gate geometric of MOSFET has become one of the most critical parameters studiedto control the device performance [13]. Two parameters included in the gate geometric are the gate length and gate width. This work is conducted to focus more on the effect of gate length on NMOS electrical characteristics such as threshold voltage.

The polysilicon depletion effect is one of the common problems that can be found due to the gate length reduction. This effect is generally a phenomenon in which an unwanted variation of the threshold voltage of the MOSFET devices using polysilicon as gate material is observed, leading to the unpredicted behaviour of the electronic circuit. It has been reported that the poly-depletion effect might degrade the gate capacitance and reduce the drain current [14] as shown in Figure 2.

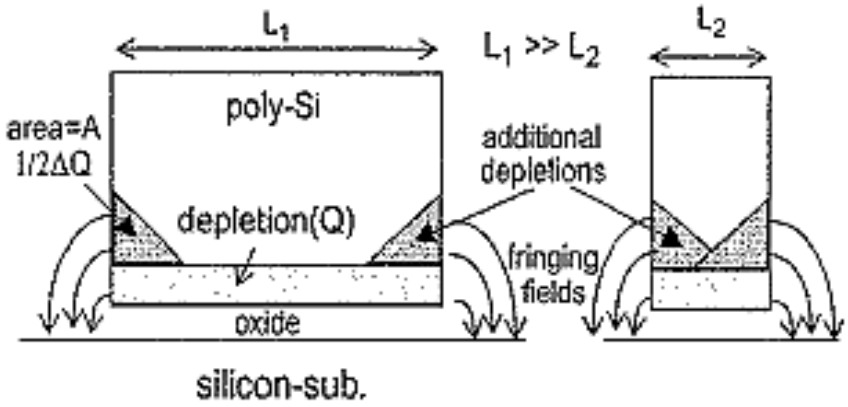

Figure 2: Gate length effect on polysilicon depletion [14].

The gate length reduction can also lead to a short channel effect. This effect occurs when the channel length is comparable to the depletion layer widths of the source and drain junctions. These effects include drain-induced barrier lowering, velocity saturation quantum confinement, and hot carrier degradation [15].

It has been studied that as the gate length is reduced, the saturated drain current, I_{Dsat} , will increase. This condition occurs because the source and drain terminals of NMOS allow bias V_{DS} to be applied across the ends of the channel region, giving rise to a drain current, I_D. Furthermore, as the gate length is scaled down, the MOS gate capacitance is degraded [16]. The degradation of the C-V characteristics can represent it.

2. METHODOLOGY

Figure 3 shows the flowchart of this project. This project only uses ATLAS tools because the polysilicon doping parameter cannot be implanted with high doping ($>10^{17}\text{cm}^{-3}$) in ATHENA tools. The process began by creating the mesh definition and fabricating the NMOS structure. It involves the creation of a silicon substrate, polysilicon gate, silicon oxide layer and aluminium contact metal region. Furthermore, this step has also defined the gate, source and drain terminal.

p-ISSN 1675-7939; e-ISSN 2289-4934

Then, the substrate and polysilicon gate were doped with the impurities. P-type impurity of 1 x $10^{18}/cm^3$ was doped in the substrate, and an n-type impurity was used for the doping process of the polysilicon gate. In this step, the concentration of n-type impurity was varied in the range of 1 x 10^{19} to 1 x $10^{21}/cm^3$ to investigate the effect of polysilicon doping on the performance of the scaled NMOS [17]. Besides, in the step of the gate terminal creation, the gate length was also varied using six different values, 0.6 μm, 0.4 μm, 0.2 μm, 60 nm, 40 nm and 20 nm. The setting of the parameters, such as polysilicon doping concentration and gate length, was shown in Table 1 and Table 2, respectively.

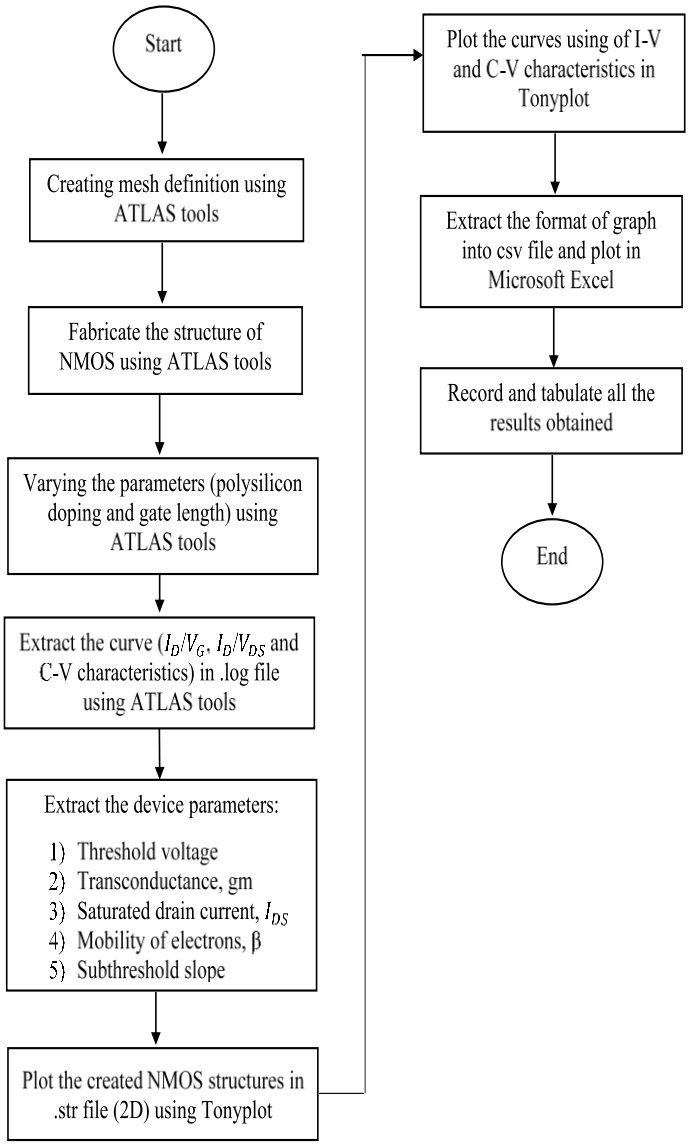

Figure 3: Flowchart of simulation process using SILVACO TCAD software.

p-ISSN 1675-7939; e-ISSN 2289-4934

Table 1: The different values of the gate length.

Size setting at the gate terminal	Length of the polysilicon gate, Lg
x-min = -0.30, x-max = 0.30	0.60 µm
x-min = -0.20, x-max = 0.20	0.40 µm
x-min = -0.10, x-max = 0.10	0.20 µm
x-min = -0.03, x-max = 0.03	60 nm
x-min = -0.02, x-max = 0.02	40 nm
x-min = -0.01, x-max = 0.01	20 nm

Table 2: The different values of polysilicon doping concentration.

Type of impurity	The concentration of doping at the polysilicon gate (cm^{-3})
n-type	1.0×10^{19}
n-type	1.0×10^{20}
n-type	1.0×10^{21}

Then, the system proceeds to the device parameter extraction and plot of the curve extraction. In order to achieve the objectives of this project, I-V and C-V characteristics curves were extracted using ATLAS tools to compare the behaviour between each parameter varied. Besides, the device parameters such as threshold voltage, transconductance, drive current, saturated drain current and mobility of electrons were also extracted using ATLAS tools. When these device parameters were collected by varying the polysilicon doping concentration, the gate length of the device was fixed at 0.4 µm and 40 nm, respectively. The reason is to compare the behaviour between the micro and nano measurements of the devices. Meanwhile, when varying the gate length of the device, the polysilicon doping concentration was fixed at 1.0×10^{20} cm^{-3} [17].

After all device parameters and the curve plot were successfully extracted, the results of the NMOS structure were simulated. Tonyplot tools plotted the characteristics curve. In this Tonyplot tool, many tools can be used to measure the parameter of the structure. More than that, the I-V and C-V curves can be extracted into 'Comma Separated Values (CSV) files and plotted in Microsoft Excel.

3. RESULTS AND DISCUSSION

3.1. Structure of NMOS with different values of gate length

Figure 4 shows the final NMOS structure constructed with 0.6 µm. The other devices have the same architecture except for the gate length, which varies according to the specified Lg mentioned in Table 1.

3.2. Variation of Polysilicon Doping Concentration

Figure 5 and Figure 6 show the I_D/V_G curve when the polysilicon doping was varied using the values of $1 \times 10^{19} cm^{-3}$, $1 \times 10^{20}\, cm^{-3}$ and $1 \times 10^{21}\, cm^{-3}$. However, these curves were extracted using the gate length of 0.4 µm and 40 nm, respectively, to observe the effect of the polysilicon doping on the large and scaled Lg devices. It can be seen that as the polysilicon doping concentration decreases, the maximum drain current, I_{ON} decreases, indicating the degradation of the current drive, which becomes more apparent [18]. The decreases in the

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polysilicon doping also lead to an increase in the threshold voltage, V_{TH} which is not suitable for low-power applications [19].

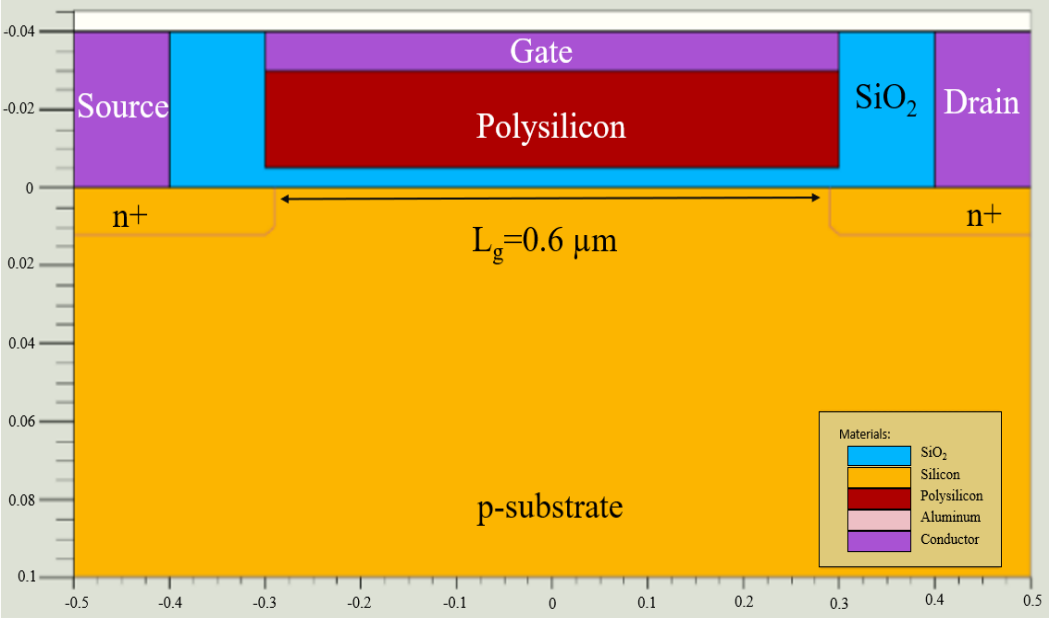

Figure 4: Final structure of NMOS with 0.6 µm gate length.

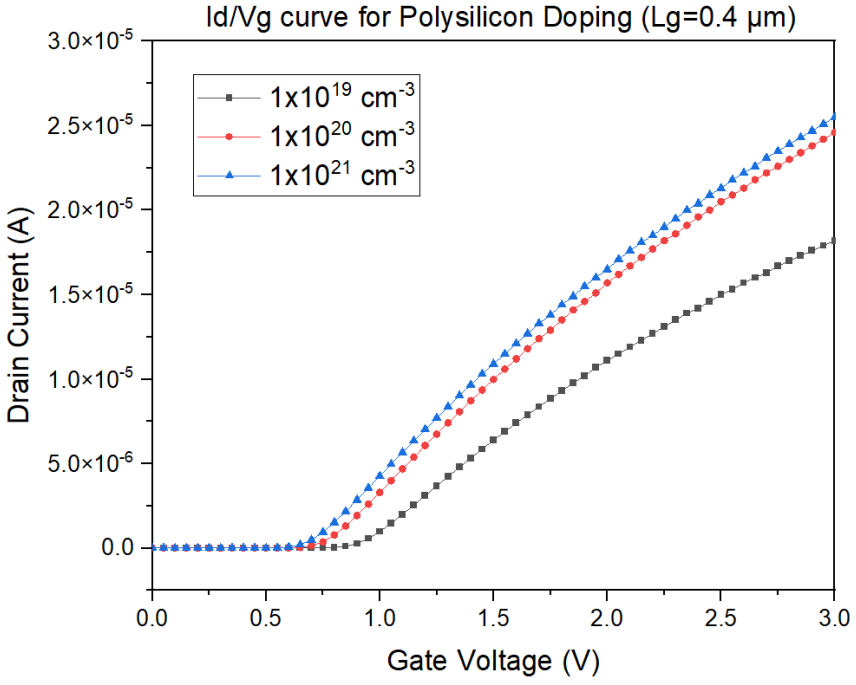

Figure 5: Id/Vg curve for three different polysilicon doping when gate length fixed at 0.4 µm.

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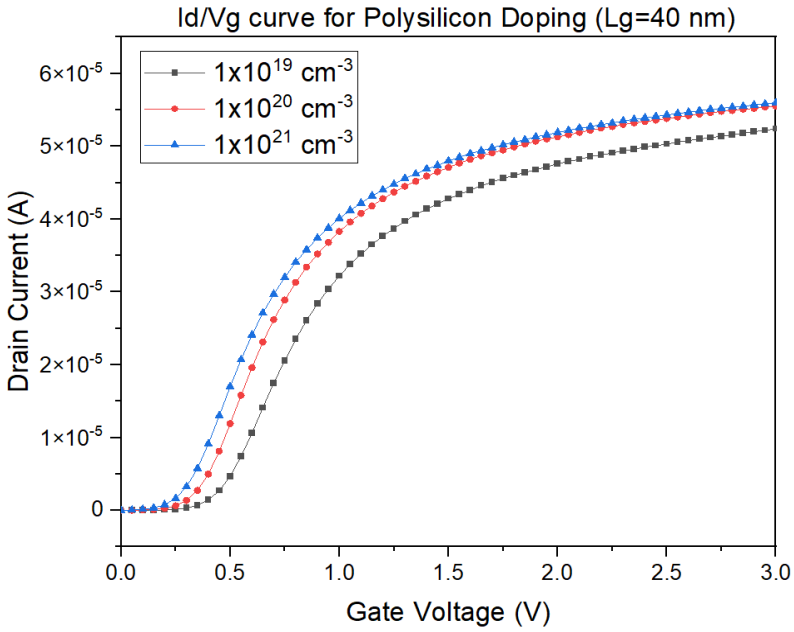

Figure 6: Id/Vg curve for three different polysilicon doping when gate length fixed at 40 nm.

Figure 7 and Figure 8 show the I_D/V_{DS} curve when the polysilicon doping was varied using the same values as the previous step. It shows that as the concentration of the doping at the polysilicon gate decreases, the I_D/V_{DS} the characteristic curve will be degraded. Reducing polysilicon doping in a MOSFET reduces the drain current, eventually degrading the current drive for the device [20].

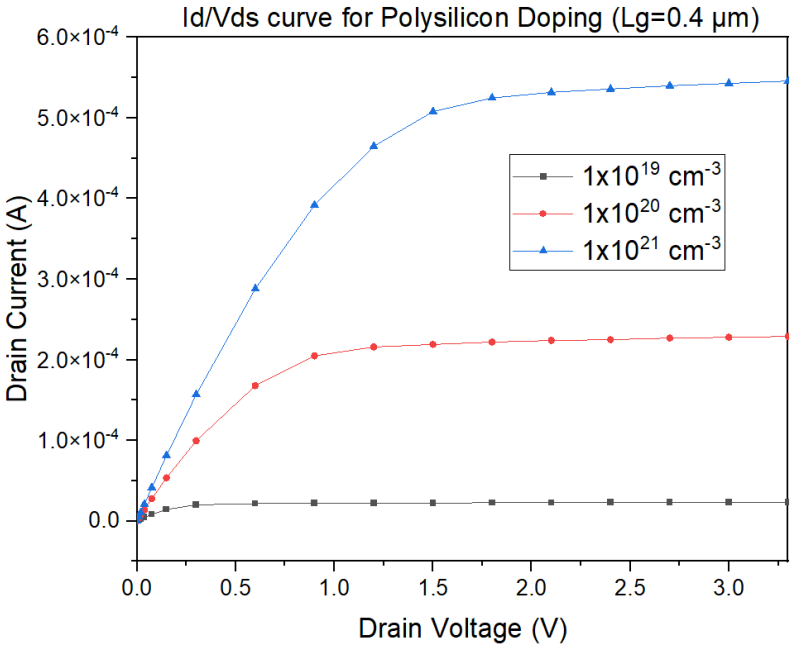

Figure 7: I_D/V_{DS} the curve for three polysilicon doping when the gate length was fixed at 0.4 µm.

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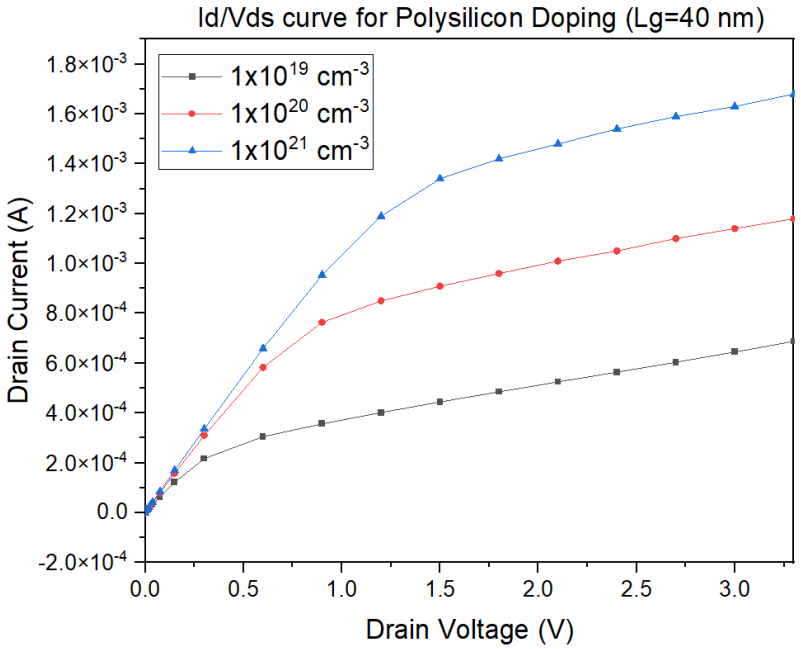

Figure 8: I_D/V_{DS} the curve for three polysilicon doping when the gate length is fixed at 40 nm.

Figure 9 shows the C-V characteristic curve when the polysilicon doping was varied. It can be seen that as the concentration of the polysilicon doping is reduced, the curve will also be degraded. The concentration of $1 \times 10^{21} cm^{-3}$ has a higher gate capacitance compared to the other concentration.

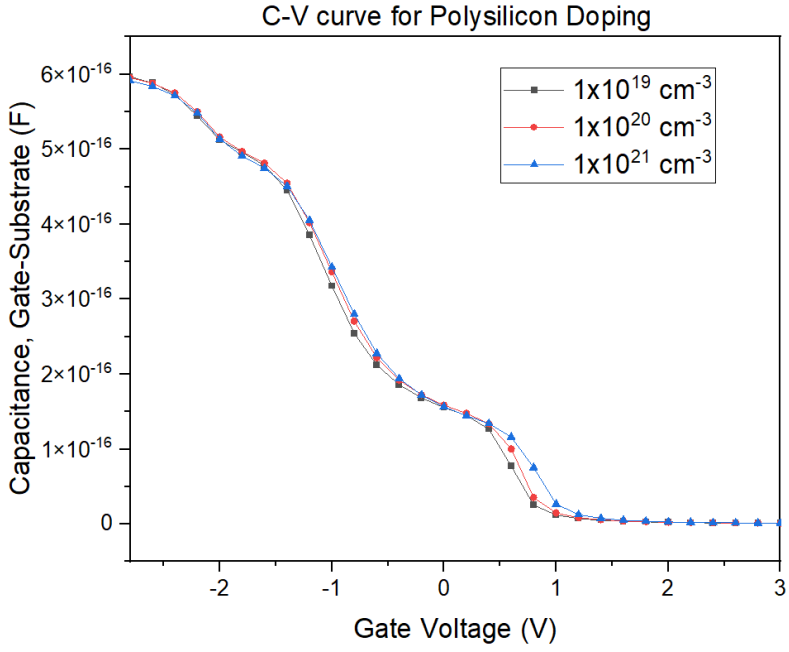

Figure 9: C-V curve for three different polysilicon doping at Lg= 40 nm.

p-ISSN 1675-7939; e-ISSN 2289-4934

Table 3 and Table 4 show the tabulation of data collected for the variation of polysilicon doping concentration using values of $1.0 \times 10^{19}\text{cm}^{-3}$, $1.0 \times 10^{20}\text{cm}^{-3}$ and $1.0 \times 10^{21}\text{cm}^{-3}$ respectively. The parameters measured including the maximum saturated drain current (I_{Dsat}), threshold voltage (V_{TH}), transconductance (gm), subthreshold slope (SS) and mobility of electron (β). During the data collection, the gate length of the device was fixed at 0.40 µm and 40 nm to compare the behaviour between the micro and nano measurements.

Table 3: Parameters extracted for the variation of polysilicon doping concentration when the gate length is fixed at 0.4 µm.

Parameters	1.0×10^{19} cm^{-3}	1.0×10^{20} cm^{-3}	1.0×10^{21} cm^{-3}
Saturated current, I_{Dsat} (A)	0.000339	0.000515	0.000546
Threshold voltage, nV_T (V)	0.81017	0.65262	0.58210
Transconductance, g_m (I/V)	6.52933×10^{-6}	9.12331×10^{-6}	9.62587×10^{-6}
Subthreshold slope (V/decade)	0.09621	0.09009	0.08976
Mobility of electrons, β	0.000225	0.000279	0.000282

Table 4: Parameter extracted for the variation of polysilicon doping concentrations when the gate length is fixed at 40 nm.

Parameters	1.0×10^{19} cm^{-3}	1.0×10^{20} cm^{-3}	1.0×10^{21} cm^{-3}
Saturated current, I_{Dsat} (A)	0.00135	0.00163	0.00168
Threshold voltage, nV_T (V)	0.18117	0.10164	0.03680
Transconductance, g_m (I/V)	0.000163	0.0001533	0.0001538
Subthreshold slope (V/decade)	0.13777	0.13112	0.13073
Mobility of electrons, β	0.001379	0.001579	0.001588

Based on the result obtained, as the concentration of the polysilicon doping is increased, the value of the threshold voltage, V_{TH} will decrease. The maximum saturated drain current, I_{Dsat} also known as drive current, I_{ON}. I_{Dsat} increases as the doping concentration increases. Hence, the poly-depletion effect can be reduced if the drive current is high. Furthermore, the saturated drain current increases as electrons mobility also increases. It can also be explained by equations (2) and (3), respectively [7];

$$I_{DS} = \beta\left(V_{GS} - V_{TH} - \frac{V_{DS}}{2}\right)V_{DS} \tag{2}$$

$$\beta = \mu_n C_{ox} \tag{3}$$

Equations (2) and (3) are defined for the I-V characteristics linear region. The drain current is directly proportional to the mobility of electrons. Besides, the increasing polysilicon doping concentration can also lead to higher transconductance. In addition, another performance parameter of the NMOS device is the subthreshold slope or SS. This value is extracted from the log scale of the I_D/V_G graph. The subthreshold current in a well-behaved MOSFET increases exponentially with V_G. The subthreshold slope, SS, as in Equation (4) [7];

$$SS = \frac{k_B T}{q}\left[\frac{d(log_{10} I_{DS})}{dV_{GS}}\right] \tag{4}$$

p-ISSN 1675-7939; e-ISSN 2289-4934

The subthreshold slope is typically quoted in millivolts per decade. The subthreshold slope is the change in gate voltage, typically quoted in millivolts needed to change the drain current by a factor of 10 [21]. The smaller the SS, the lower the gate voltage needed to switch the transistor from the OFF to ON state. Besides, the subthreshold slope decreases as the polysilicon doping concentration increases. Hence, the lower subthreshold slope indicates better channel control, improved I_{ON}/I_{OFF} ratio, less leakage and less energy.

3.3. Variation of Gate Length

Figure 10 shows the I_D/V_G the curve of the NMOS when the gate lengths were varied as Lg1 = 0.6 µm, Lg2 = 0.4 µm, Lg3 = 0.2 µm, Lg4 = 60 nm, Lg5 = 40 nm and Lg6 = 20 nm respectively. It can be observed that as the gate is scaled down, the drain current will be increased. This condition occurs because the source and drain terminals of NMOS allow bias V_{DS} to be applied across the ends of the channel region, giving rise to a drain current, I_D. The gate length of 20 nm has the highest drain current compared to other gate lengths; however, it suffers from higher I_{off} or leakage current.

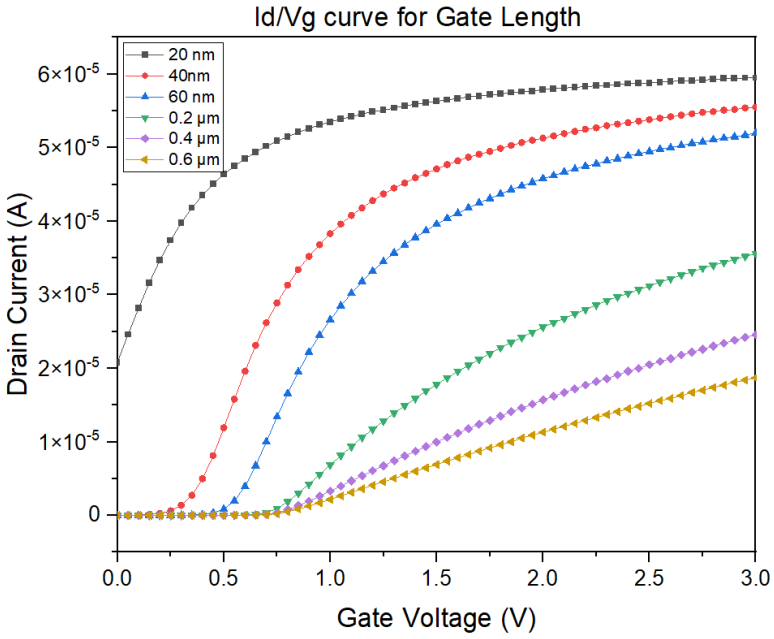

Figure 10: I_D/V_G the curve for six different gate lengths of polysilicon doping was fixed at 1.0 $\times 10^{20}$ cm^{-3}.

Figure 11 shows the I_D/V_{DS} the curve of the NMOS when the gate lengths were varied using the same values as the previous step. It can be seen that the drain current increases linearly when the drain voltage starts to increase, and it reaches the saturation point when $V_D = V_{Dsat} = V_G - V_t$. This is the point where I_{Dmax} is reached. The drain current then saturated when the $V_D > V_{Dsat}$. However, the graph shows that the drain current still increases when the drain voltage increases. This is due to the channel length modulation effect [22]. The effect is more pronounced for the lower Lg, where the slope of I_D is greater. The graph also shows that as the gate length is reduced, the I_{Dmax} increases.

p-ISSN 1675-7939; e-ISSN 2289-4934

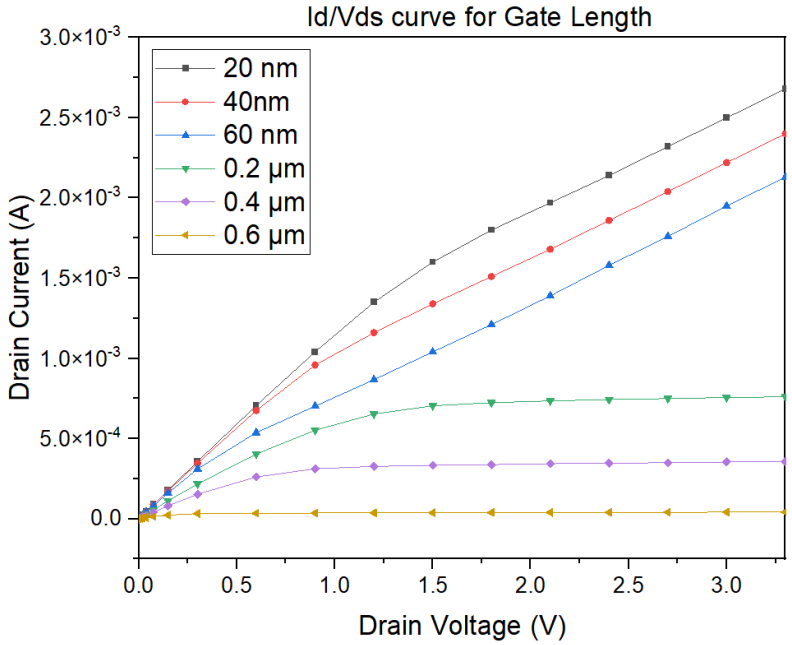

Figure 11: I_D/V_{DS} the curve for six different gate lengths concentration of polysilicon doping was fixed at 1.0×10^{20} cm^{-3}.

Table 5 shows the tabulation of data collected for the variation of gate length of NMOS using values of 0.6 µm, 0.4 µm,0.2 µm, 60 nm, 40 nm and 20 nm, respectively. During the process of the variation of this parameter, the concentration of polysilicon doping was fixed at 1.0×10^{20} cm^{-3}.

Table 5: Data collected for the variation of gate length

Parameters	0.6 µm NMOS	0.4 µm NMOS	0.2 µm NMOS	60 nm NMOS	40 nm NMOS	20 nm NMOS
Saturated current, I_{Dsat} (A)	0.000389	0.000515	0.000761	0.001321	0.001634	0.002675
The threshold voltage, nV_T (V)	0.66895	0.65262	0.60716	0.35534	0.10164	0.09183
Transconductance, g_m (A/V)	5.5667×10^{-6}	9.1233×10^{-6}	1.8682×10^{-5}	8.6769×10^{-5}	0.000176	0.000576
Subthreshold slope (V/decade)	0.08997	0.09009	0.09072	0.10497	0.13112	0.68803
Mobility of electrons, β	0.000194	0.000279	0.000521	0.001349	0.001579	0.001515

Based on the result obtained in Table 5, it can be observed that as the gate length is reduced, the threshold voltage, nV_T will be reduced. The 0.20 µm length of the polysilicon gate has the lowest threshold voltage compared to the other gate length. Furthermore, the saturated drain current will increase. This hypothesis can be proven by relating the theory presented by equation (5) [7];

p-ISSN 1675-7939; e-ISSN 2289-4934

$$I_{Dsat} = \frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2 \quad (5)$$

Based on equation (5), I_{Dsat} is inversely proportional to the gate length. Hence, the gate length of 20 nm has the highest saturated drain current; thus, it might reduce the polysilicon depletion effect in a scaled NMOS structure. However, the subthreshold slope will increase. This may be since the capability of the device to control the circuit system might be reduced when the small gate length is used. The leakage current might also be increasing due to the situation. Furthermore, the transconductance and mobility of electrons will increase as the gate length is reduced.

Based on the simulation and data collected, it can be concluded that the optimum concentration of polysilicon doping that can reduce the poly-depletion effect is 1.0×10^{21} cm^{-3}. Besides, the optimum gate length that can be used to overcome that problem is 20 nm. The reason why these values are chosen is the high drive current of the transistor obtained during both of the simulations.

4. CONCLUSION

In conclusion, this project was successfully carried out to investigate the effect of geometric gate effect and polysilicon doping on the performance of scaled NMOS. This project has been done by using SILVACO TCAD software. The aim of this project has been achieved as the optimum gate length and polysilicon doping concentration to overcome the problem of the poly-depletion effect wassuccessfully obtained. The gate lengths were varied using six different values, which are 0.6 µm, 0.4 µm, 0.2 µm, 60 nm, 40 nm and 20 nm. At the same time, the behaviour between the micro and nano measurements in the gate length has been analysed. Meanwhile, the poly-doping concentrations were varied using the values in the range of 1 x 10^{19} to 1 x $10^{21}/cm^3$. It can be concluded that the optimum concentration of polysilicon doping and gate length to reduce the problem of the poly-depletion effect is $1.0 \times 10^{21} cm^{-3}$ and 20 nm, respectively. This is because the device parameters such as saturated drain current, transconductance, threshold voltage, subthreshold slope and mobility of electrons had achieved the best condition when using those optimum gate lengths and polysilicon doping concentration.

ACKNOWLEDGEMENT

The author wishes to thank members of Universiti Teknologi MARA, Pulau Pinang Branch, USM, and Department of Applied Science, Universiti Teknologi MARA, Pulau Pinang Branch, for their unwavering technical assistance. The financial support from the Universiti Teknologi MARA through MyRA Research Grant Scheme (600-RMC/GPM ST 5/3 (042/2021) and Universiti Teknologi MARA, Cawangan Pulau Pinang is gratefully acknowledged.

CONFLICT OF INTEREST

The authors declare that there is no conflict of interest regarding the publication of this paper.

p-ISSN 1675-7939; e-ISSN 2289-4934

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