UNIVERSITI TEKNOLOGI MARA

DESIGN OF SERIAL PERIPHERAL INTERFACE WITH FLEXIBLE MODES AND FREQUENCY FOR ADVANCED MICROCONTROLLER BUS ARCHITECTURE-ADVANCED PERIPHERAL BUS INTERFACE

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ABSTRACT

The model and design of the intellectual property (IP) core of serial peripheral interface (SPI) with Advanced Microcontroller Bus Architecture (AMBA) – Advanced Peripheral Bus (APB) interfacing are presented. The objectives of the project are to model and design a SPI that is interfacing with IP core of APB for sending and receiving data from a single slave to model APB-SPI controller with controllable data and designed with maximum operating frequency of 16 MHz and flexibility in all four clocking modes and finally to synthesize and validate the model of the SPI design. For this work, research regarding interfacing SPI with another core and designing the SPI itself is essential for the project. The design and simulation of SPI master and slave is based on Verilog coding. The Verilog code is the main language that is use for designing and running simulations for this project. SPI is one of the commonly used serial protocols that can send or receive data from a single or multi-slave. Due to proliferation of communication protocols and requirement of flexibility in communication, this work shows how an architecture of APB-SPI controller with controllable data width and an operating frequency of 16MHz is designed. The SPI is simulated, verified, synthesized, carry a layout design and routed using tools such from the electronic design automation (EDA) tools which is Synopsys, simulation software which are ModelSim and Quartus prime lite. The design and implementation of SPI model interface is targeted to be used in Low Power Wireless Microcontroller Unit and its specification is based on Nordic Wireless RF System on Chip. The modes of SPI also play important role in this work where this protocol can run through four modes that corresponds to four possible clocking configurations. The results showed that the core of SPI was successfully modelled and designed with maximum operating frequency of 16 MHz and flexibility in all four clocking modes. The ASIC design of this work consumed an area of 27750 μm2 and a power of 47.12μW by using Silterra 0.18μm for future fabrication CMOS process.

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