Single Phase Matrix Converter for Boost Inverter Operation Controlled Using Xilinx FPGA

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Abstract— **This paper is concerned on FPGA design for control implementations of the Single Phase Matrix Converter (SPMC) operating as a Boost Inverter. The main attribute of the boost inverter topology is the fact that it generates an ac output voltage larger than the dc input voltage depending on the instantaneous duty cycle. The power circuit uses the Insulated Gate Bipolar Transistor (IGBT) as switching device in the SPMC implementation. The Sinusoidal Pulse Width Modulation (SPWM) technique is used to synthesize the output voltage. The selected experimental and simulation results are presented to verify the proposed operation of boost inverter.**

Keywords: Boost Inverter; Single Phase Matrix Converter (SPMC); Sinusoidal Pulse Width Modulation (SPWM); Field Programmable Gate Array (FPGA); Insulated Gate Bipolar Transistor (IGBT).

I. INTRODUCTION

Single phase voltage source inverters are widely used for example in shunt active power filter applications for energy transformation [1, 2] where bidirectional operation is required. Alternative topologies such as matrix converters present future potential and are an emerging research topic. It is an advanced converter known to offer an "all silicon" solution for direct AC-AC conversion as introduced by Gyugyi [3], mainly with three-phase circuit topologies [4,5]. The single-phase version has recently emerged with works on AC-AC [6, 7], DC-DC [8], DC-AC conversion [9] and most recently the AC-DC rectifier [10]. However limited knowledge on its control and safe-commutation [11] has limited its use in applications.

This paper will discuss the design and development of a pulse-width modulation (PWM) generator suitable for Single-Phase Matrix Converter (SPMC) operating as a boost inverter. It is based on the Xilinx chip XC4005XL Field Programmable Gate Array (FPGA) with IGBTs as the power switching device. The output voltage of the circuit is synthesized using Sinusoidal Pulse Width Modulation (SPWM). The proposed design enables the modulation index and the switching frequency to be changed externally. Results are provided to demonstrate successful implementation of the design. Prior to hardware implementation, simulations were performed to predict the behavior. A laboratory model test-rig of the SPMC was the constructed to experimentally verify the result.

II. SINGLE PHASE MATRIX CONVERTER

The Single Phase Matrix Converter (SPMC) that is used in direct AC-AC converter that requires four-bidirectional switches that capable of blocking voltage and conducting current in both directions as shown in Figure 1. In the absence of discrete semiconductor device that could fulfill the needs, hence the use of common emitter anti-parallel IGBT, diode pair is used. IGBTs are used due to its popularity among researchers that could lead to medium-power applications. It is a robust switching device with reasonably fast switching frequency suitable during research and investigations due to the presence of switching spikes inherent in any Matrix Converter when feeding inductive loads.

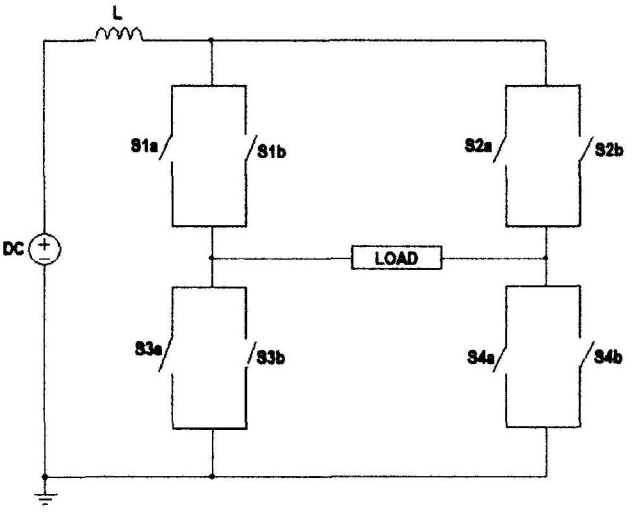

Figure 1: Single Phase Matrix Converter (SPMC) topology.

The circuit comprises four bidirectional switches, which is S1, S2, S3, and S4 capable of conducting current in directions, blocking forward and reverse voltage (symmetrical devices) and switching between states without any delays.

III. CONVENTIONAL INVERTER

When an output voltage larger than the input one is needed, a boost dc-dc converter must be used between the dc source and inverter as shown in Figure 2.

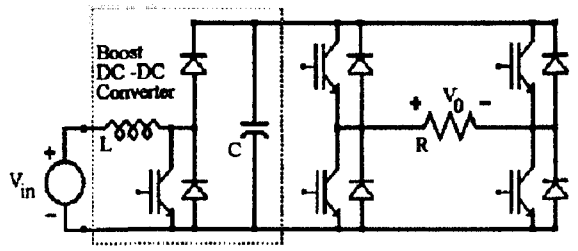

Figure 2: Circuit used to generate an ac voltage larger than the dc input voltage.

The proposed boost inverter achieves dc-ac conversion, as indicated in Figure 3, by connecting the load differently across two dc-dc converters and modulating the dc-dc converter sinusoidal output voltages. The blocks A and B represent dc-dc converters. These converters produce a dc-biased sine wave output, so that each source only produces a unipolar voltage. The modulation of each converter is 180^0 out of phase with the order, which maximizes the voltage excursion across the load. Thus, whereas a dc bias appears at each end of the load, with respect to ground, the differential dc voltage across the load is zero. The generating bipolar voltage at output is solved by a push-pull arrangement. Thus, the dc-dc converters need to be current bidirectional.

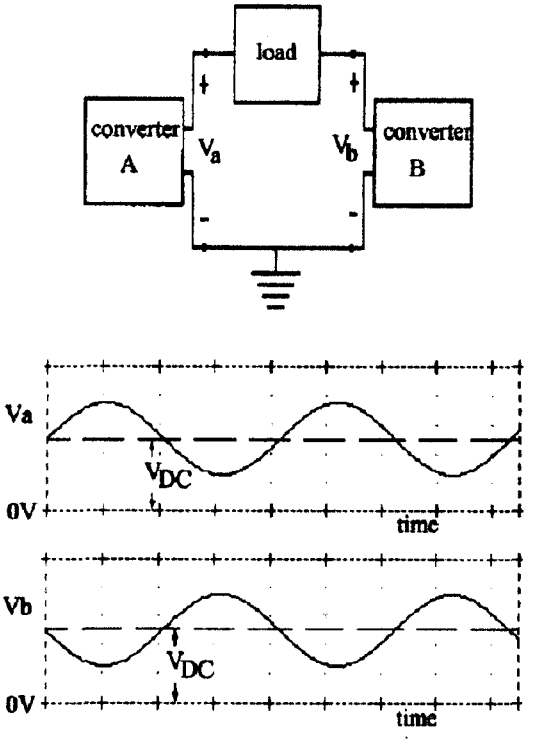

Figure 3: A basic approach to achieve dc-ac conversion, with boost characteristics.

The current bidirectional boost dc-dc converter is shown in Figure 4. A circuit implementation of the boost inverter is shown in Figure 5. For a dc-dc boost converter, by using the averaging concept, we obtain the voltage relationship for the continuous conduction mode given by

$$\frac{V1}{Vin} = \frac{1}{1-D}$$

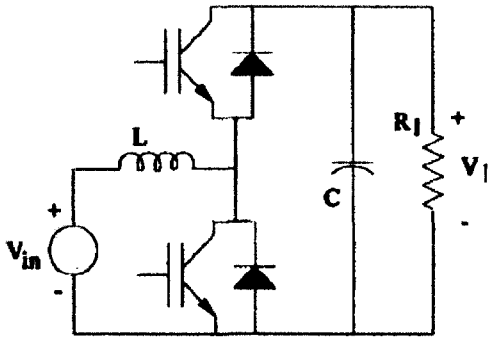

Figure 4: The current bidirectional boost dc-dc converter.

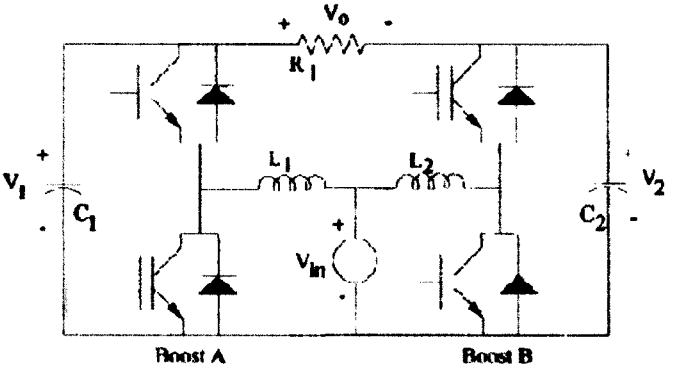

Figure 5: The dc-ac boost converter.

where D is the duty cycle. The voltage gain for the boost inverter can be derived as follows: assuming that the two converters are 180^0 out of phase, then the output voltage is given by

$$Vo = V1 - V2 = \frac{Vin}{1-D} - \frac{Vin}{D}$$

$$\frac{Vo}{Vin} = \frac{2D-1}{D(1-D)}$$

IV. PROPOSED SPMC

The switching sequence for operation of SPMC as an inverter as shown in Figure 6, for an output of 50Hz is tabulated in Table I, illustrated in terms of circuit current flows as in Figures 7 and 8 with its switching sequence for an output frequency of 50Hz.

The boost inverter includes dc supply voltage V_{in}, boost inductor, power switches IGBTs S_1-S_4, filter capacitor and inductor, free-wheeling diodes D_1-D_4, and load resistance R.

In Figure 7, the bold-line represents the control (SPWM) switch and the dotted line represents the current flow for commutation switches. Similar illustration is used in Figure 8. The switching sequence of boost inverter need to be developed as illustrated in Figures 9 and 10 to allow force controlled freewheeling diode.

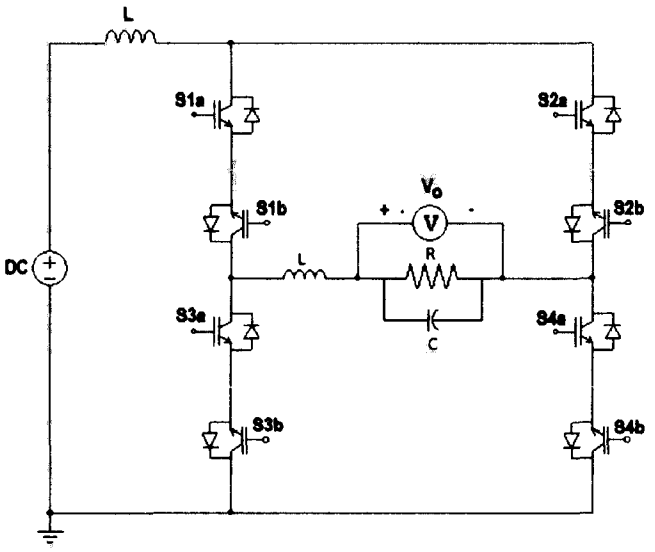

Figure 6: Proposed boost inverter using SPMC with LC filter.

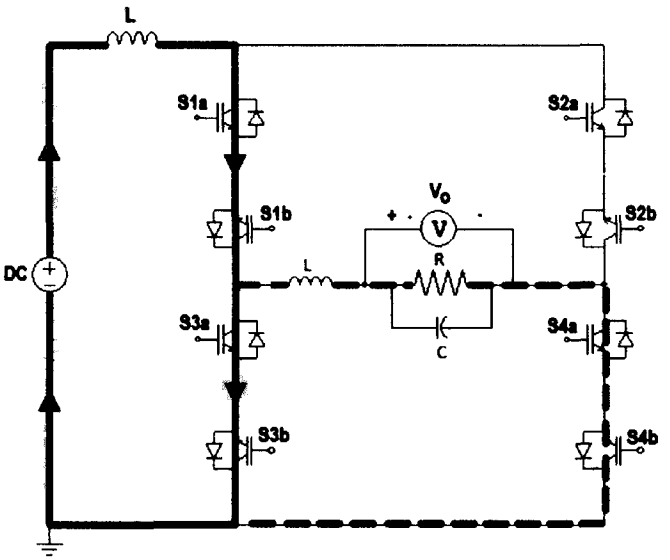

Figure 7: Positive cycle of boost inverter.

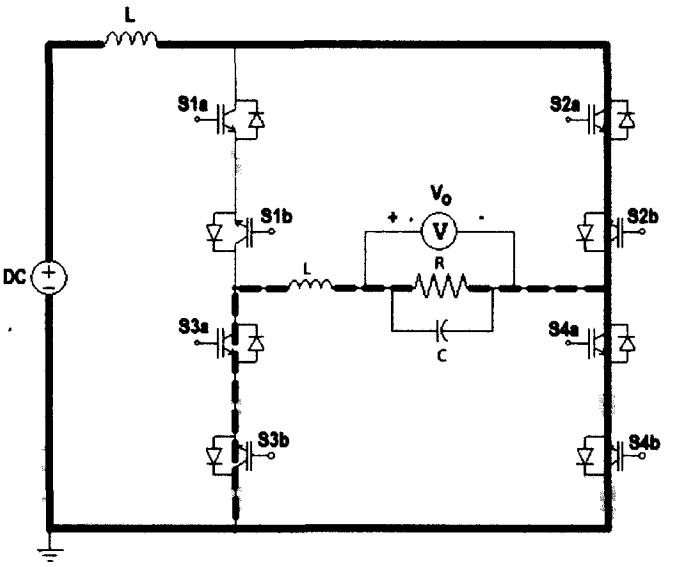

Figure 8: Negative cycle of boost inverter.

Table I: Switching strategies of Boost Inverter

Switches	Operation	
	Positive Cycle	Negative Cycle
S1a	PWM	Off
S1b	Off	Off
S2a	Off	PWM
S2b	Off	Off
S3a	PWM	On
S3b	Off	Off
S4a	On	PWM
S4b	Off	Off

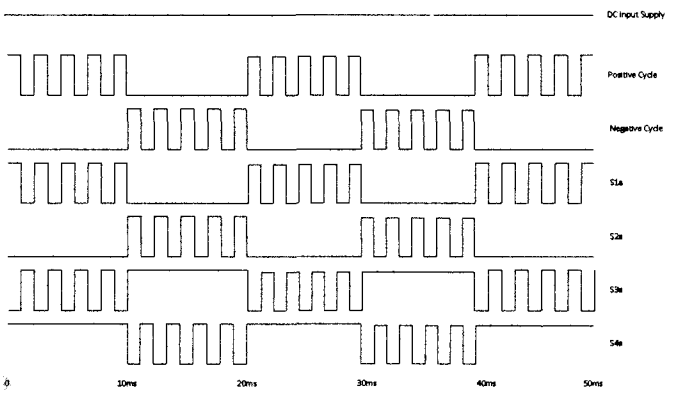

Figure 9: Switching algorithm for commutation strategy.

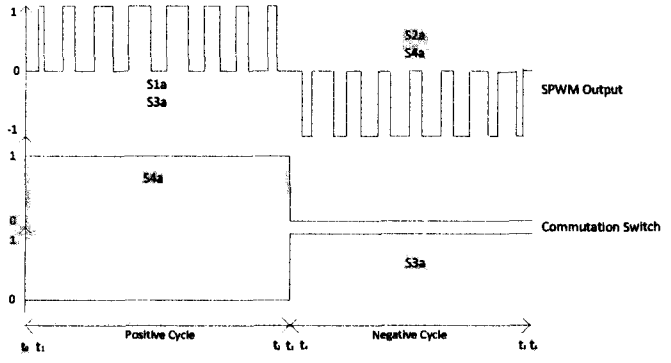

Figure 10: Switching pattern of boost inverter.

One complete switching cycle (positive and negative cycle) is divided into six states described as follows;

Step 1: (t_0~t_1) at time t_0, S4a is turned ON provided the overlap period prior to S1a and S3a being switched with PWM control.

Step 2: (t_1~t_2) at time t_1, control (SPWM) switches S1a and S3a are turned ON (after delay time). During this period, current flows into the inductive load (energized) through S1a and left to be dissipated (de-energized) through S4a when S3a is turned OFF.

Step 3: (t_2~t_3) at time t_2, control (PWM) S3a is turned OFF and the inductive load is de-energized during overlap period between S3a and S4a being active.

Step 4: (t_3~t_4) at time t_3, S3a is turned ON to provide an overlap period prior to S2a and S4a being switched with PWM control.

Step 5: (t_4~t_5) at time t_5, control (SPWM) switch S2a is turned ON (after delay time). This operates in a similar manner to step 2.

Step 6: (t_5~t_6) at time t_5, S4a is turned OFF. A complete cycle is ended to complete a switching cycle.

V. Modeling And Simulation

The proposed control concept is verified through simulation using MATLAB/Simulink (MLS) with SimPowerSystems to study the behavior of boost inverter operation. Figure 11 shows the modeling of SPMC and Controller which is to operate as boost inverter with its switching sequence as shown in Table I. Subsystem is used by breaking up large model into a hierarchical set of smaller models as shown in Figure 12 to Figure 14. Top model of SPMC shown in Figure 11 consists of four bidirectional switch and each switch have a diode pair and IGBTs as illustrated in Figures 12 and 13.

The controller unit implements the operation of boost inverter using SPMC is as shown in Figure 14. For the former, the sine wave is compared to zero using "Compare to Zero" function producing an 'ON' pulse for positive cycle operation. A constant representing a reference signal used vary the modulation index which is compared with the carrier signal (triangular waveform) from "Repeating Sequence" block to produce the required respective PWM output signal. This is implemented using the "Relational Operator" block. Then the signal made synchronous to the PWM signal using gate logic 'OR' block set to obtain the desired output signal (Figure 9).

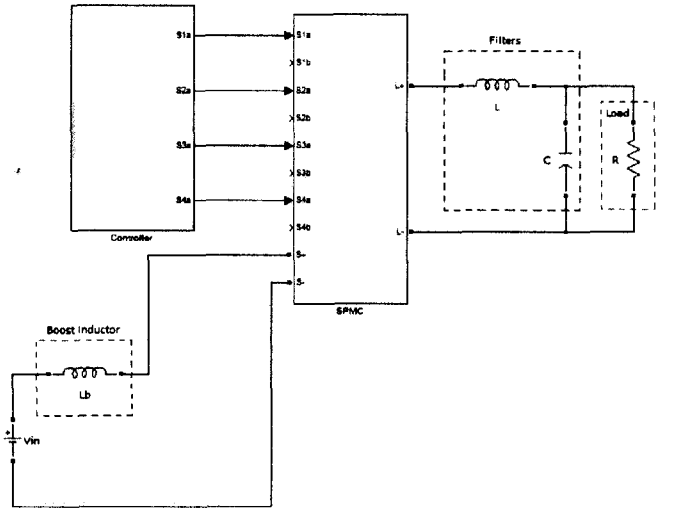

Figure 11: Modeling of Boost Inverter in MATLAB/Simulink.

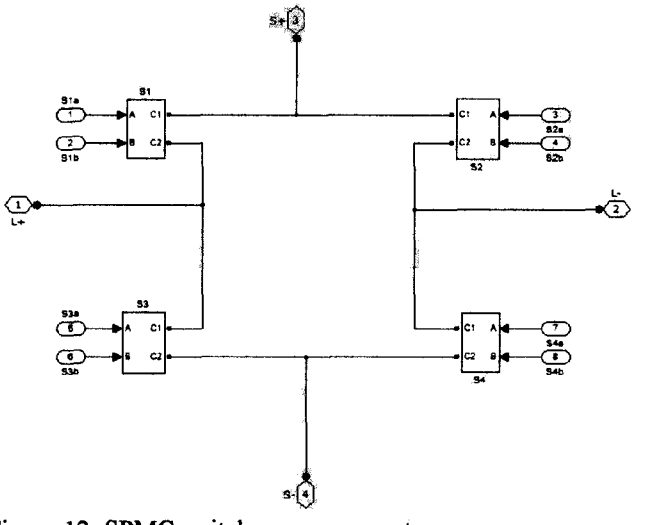

Figure 12: SPMC switches arrangement.

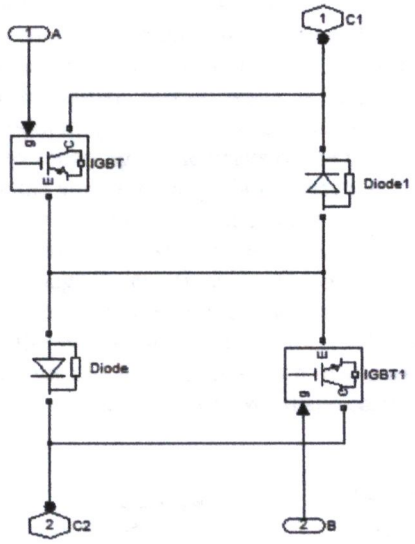

Figure 13: Bidirectional switches with diode pair.

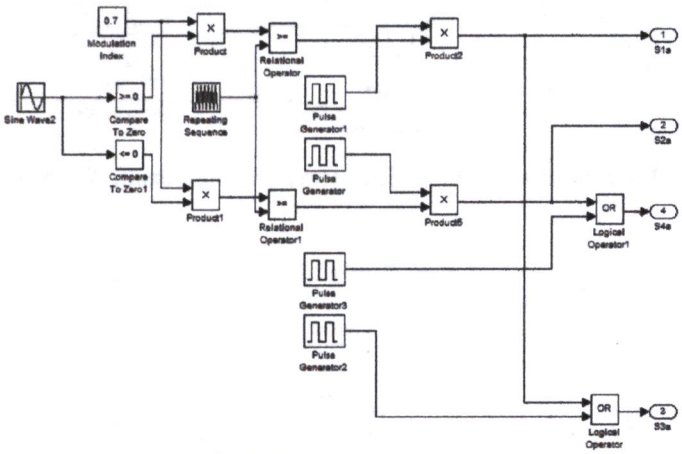

Figure 14: Controller unit for Boost Inverter.

VI. FPGA IMPLEMENTATION

The overall block diagram of the SPWM generator for boost inverter operation in Xilinx FPGA is as shown in Figure 15. The top level of Xilinx FPGA schematic diagram is as shown in Figure 16. There are a few major components, namely as

- External Main Clock
- 'W' shape carrier signal
- Comparator
- Multiplier
- Modulation index
- ROM
- Memory pointer

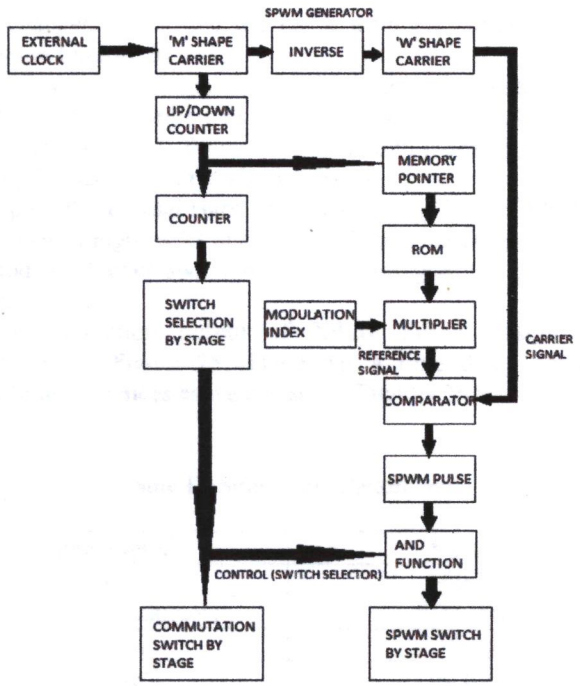

Figure 15: FPGA SPWM Generation Algorithm for Boost Inverter Operation.

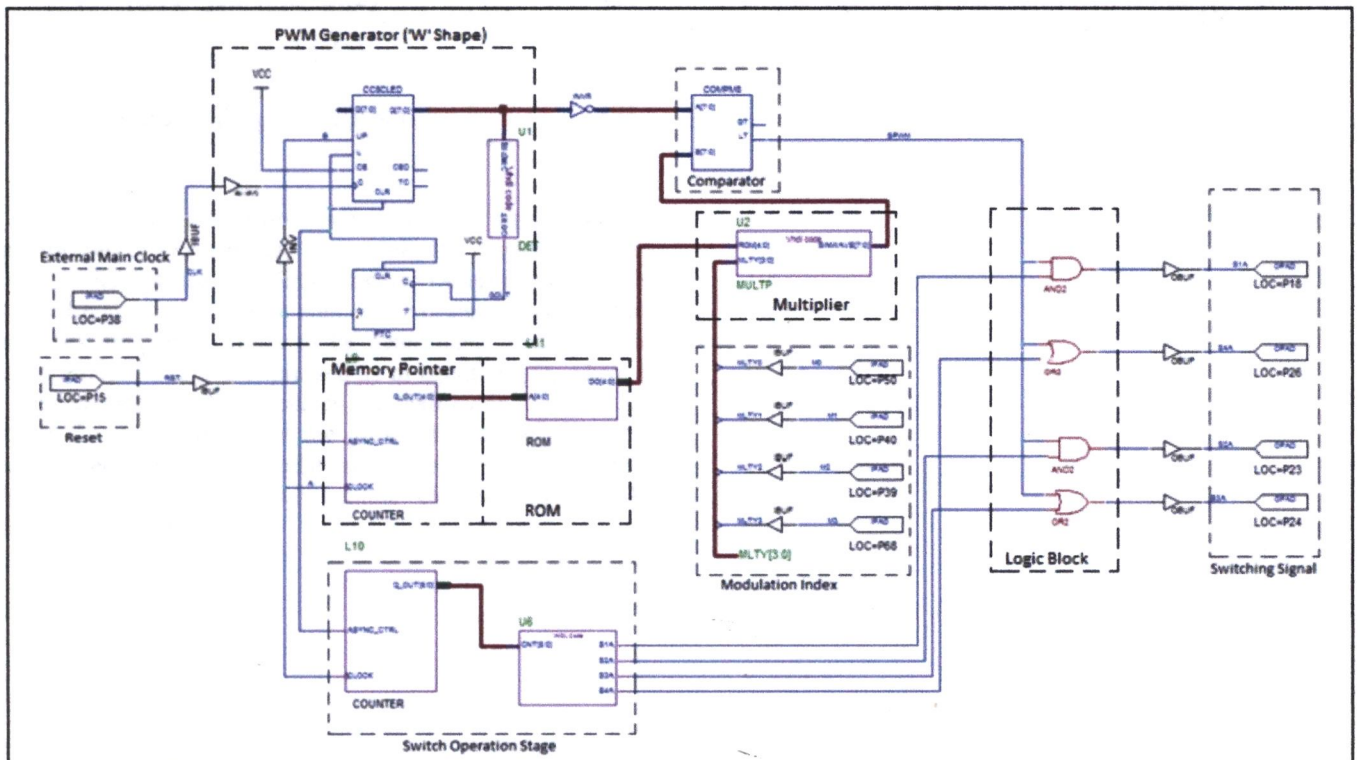

Figure 16: Schematic diagram of Xilinx FPGA.

The developed PWM signal is based on symmetrical PWM, a modified technique of a natural sampling PWM suitable for digital implementation. In Sinusoidal Pulse Width Modulation (SPWM), a triangular carrier wave is use to sample the sinusoidal modulating wave once every carrier cycle at regular intervals, corresponding to the peaks of the triangular wave. It is to produce the amplitude modulation wave, m_a.

The real time generation of sine wave value is stored in a look-up table inside ROM, where the values are first pre-determined through calculations using equation (1) and (2). Comparison of both waves defines the intersection point used to determine the switching instants of the PWM, defined as in equation (3) with illustrations as shown in Figure 16. An up-down counter is used to generate 'W' shape carrier signal.

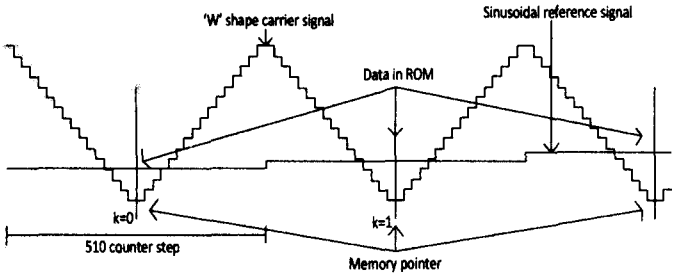

Figure 17: Illustration of memory pointer and data from ROM.

$$V_{ref}(t_k) = \text{round}\,[25.5\sin(2\pi 50 t_k)] \quad (1)$$

$$t_k = (2k+1)\left(\frac{T_{carrier}}{2}\right) \quad (2)$$

$$t_{step} = \frac{T_{carrier}}{step_{total}} = \frac{T_{carrier}}{510} \quad (3)$$

$$T_{carrier} = \frac{T}{2N} \quad (4)$$

$$f_{clock} = f_{carrier}(2^n-1)(2) \quad (5)$$

$$step_{total} = (2^n-1)(2) \quad (6)$$

$$T_c = (step_{total})(T_{clock}) = step_{total}\left(\frac{1}{f_{clock}}\right) \quad (7)$$

The rate at which the up-down counter for carrier wave is incremented or decremented determines the carrier frequency and accuracy of the sampling process. Determination of the carrier frequency is the first step of the design process, where the clock frequency needs to be determined precisely. The carrier period, $T_{carrier}$ is expressed as in equation (4), where N is the number of carrier pulses per half-cycle, $f_{carrier}$ is the carrier frequency and T is the period for modulation. The carrier frequency has a relationship with the main clock frequency and the up-down counter can be expressed by equations (5), (6) and (7).

From Figure 15, an external main clock input was used as the clocking signal for the FPGA counter for various carrier signals. The multiplier (MULTP) block as shown is created using VHDL used to multiply the external source data (Modulation Index) with the data stored in ROM (reference sine-wave). The modulation index is set by using 4-bit external data. The magnitude of sine-wave is obtained by multiplying the input from external data.

VII. Results And Discussions

Modulation index, $m_a = 0.7$ was used for the simulation in MATLAB/Simulink (MLS) and other parameters as in Table II. The result from the simulation output voltage and current was presented in Figures 18 and 19. Modulation index, m_a was changed to 1.0 and the result from the simulation was shown in Figures 20 and 21.

Analysis of the output voltage, V_o against modulation index, m_a for SPMC supplied by input voltage, V_{in} = 100 V was shown in Figure 22. When the modulation index, m_a increase to 1.0, the output voltage also increases.

A plot of the Total Harmonic Distortion (THD) of SPMC is as shown in Figures 23 and 24. The higher modulation index, m_a and the higher switching frequencies give the best THD value.

The simulation output of Xilinx FPGA design was illustrated in Figure 25. There has a time delay between switching sequences as we can see in Figures 26 and 27.

Table II: Simulation Parameters

Parameter	Value
V_{in}	100 V
L_B (Boost Inductor)	0.04 mH
L (filter)	0.55 mH
C (filter)	60 µF
R	120 Ω
f_s	5 kHz
f	50 Hz

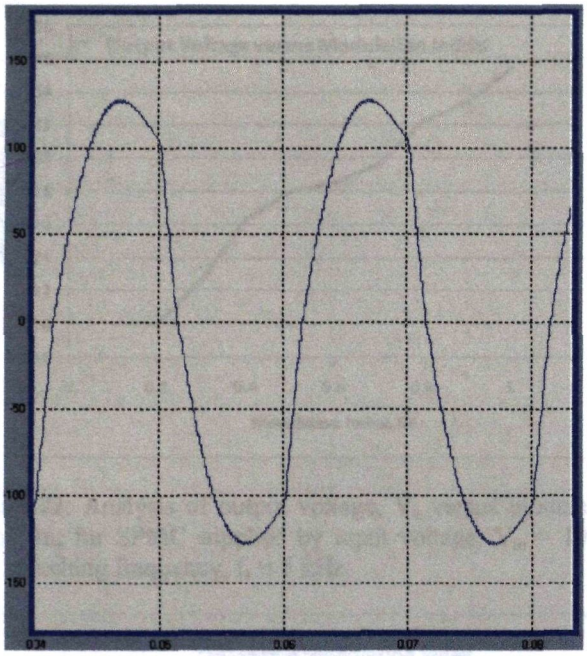

Figure 18: Simulation output voltage of R load (MLS) for modulation index, $m_a = 0.7$.

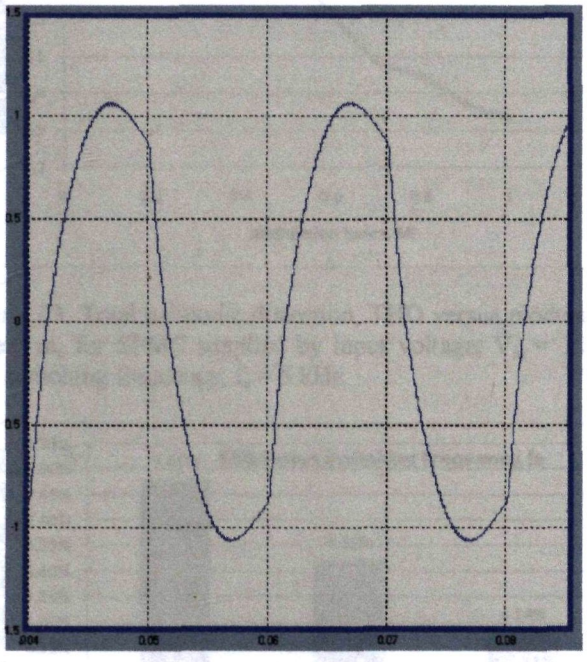

Figure 19: Simulation output current of R load (MLS) for modulation index, $m_a = 0.7$.

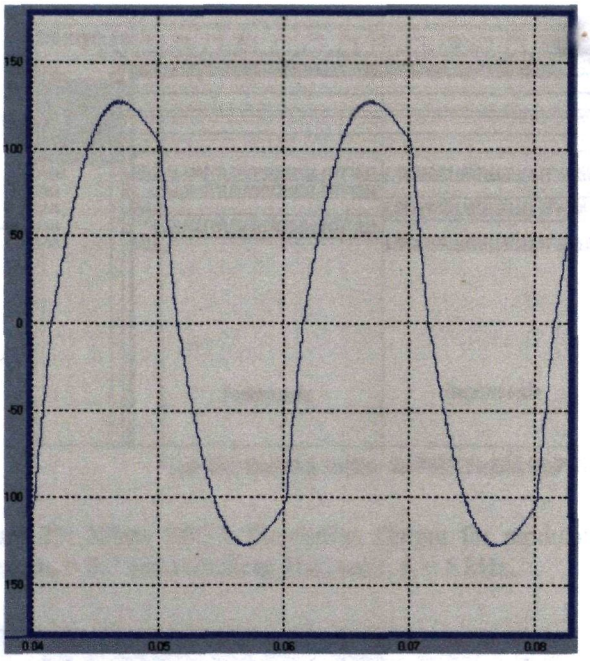

Figure 20: Simulation output voltage of R load (MLS) for modulation index, $m_a = 1.0$.

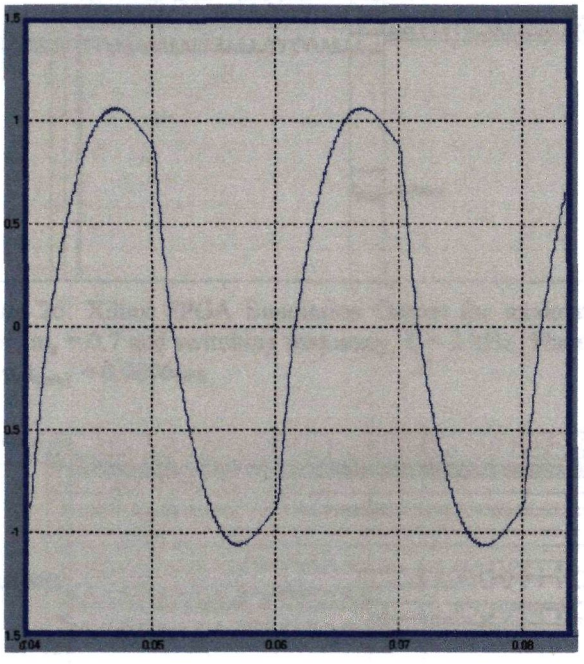

Figure 21: Simulation output current of R load (MLS) for modulation index, $m_a = 1.0$.

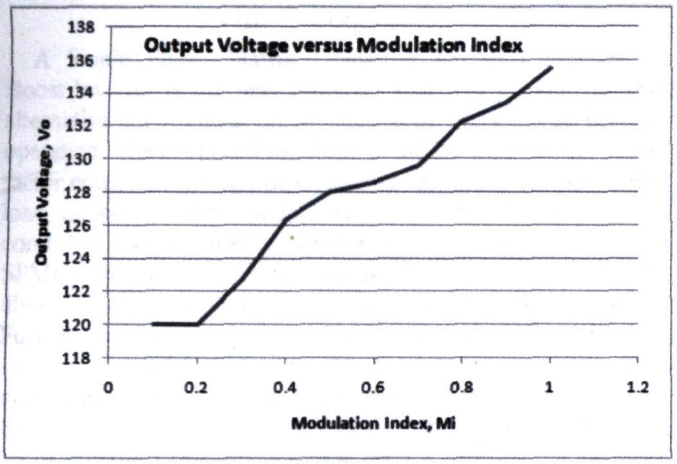

Figure 22: Analysis of output voltage, V_o versus modulation index, m_a for SPMC supplied by input voltage, V_{in} = 100 V and switching frequency, f_s = 5 kHz.

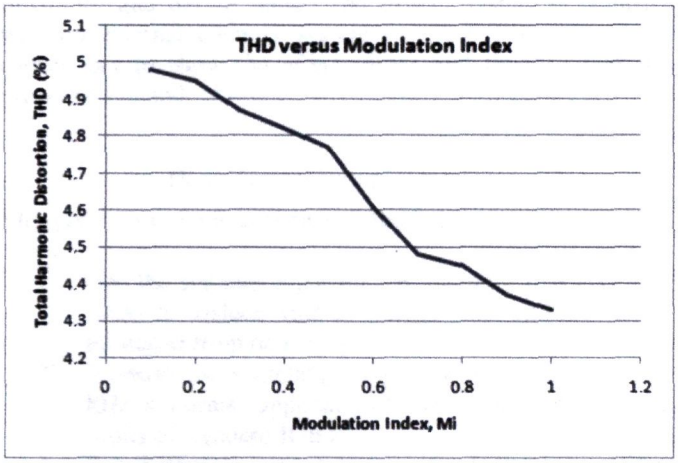

Figure 23: Total harmonic distortion, THD versus modulation index, m_a for SPMC supplied by input voltage, V_{in} = 100 V and switching frequency, f_s = 5 kHz.

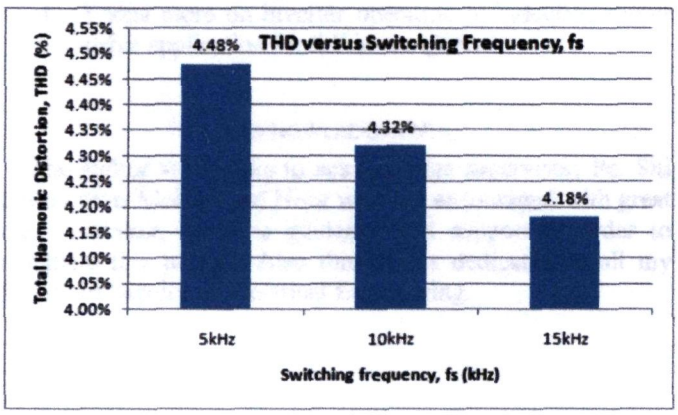

Figure 24: Total harmonic distortion, THD versus switching frequency, f_s for SPMC supplied by input voltage, V_{in} = 100 V and modulation index, m_a = 0.7.

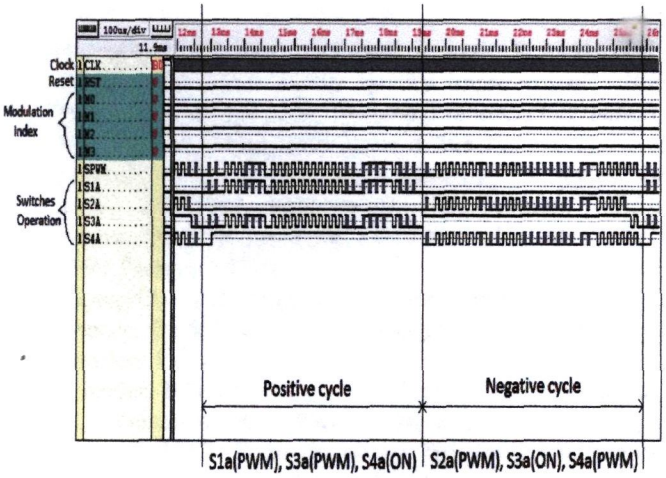

Figure 25: Xilinx FPGA Simulation Output for modulation index, m_a = 0.7 and switching frequency, f_s = 5 kHz.

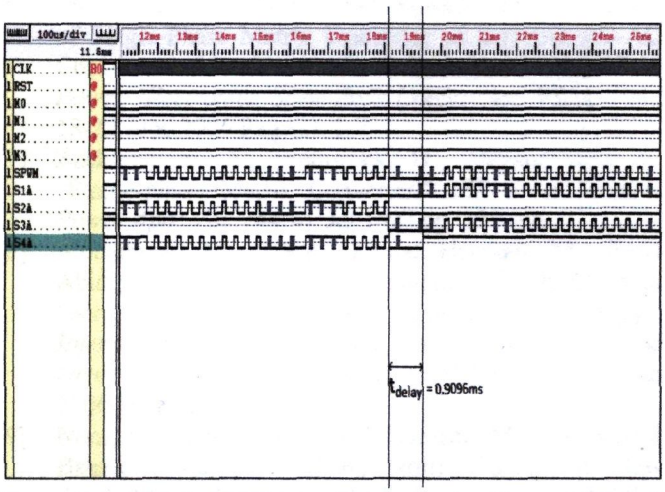

Figure 26: Xilinx FPGA Simulation Output for modulation index, m_a = 0.7 and switching frequency, f_s = 3 kHz. The time delay, t_{delay} = 0.9096ms.

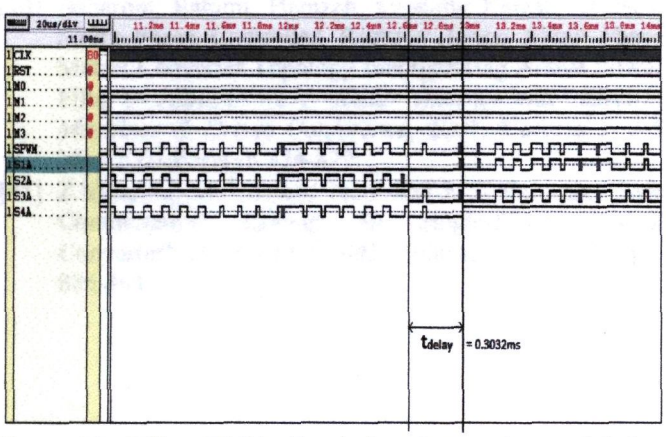

Figure 27: Xilinx FPGA Simulation Output for modulation index, m_a = 0.7 and switching frequency, f_s = 6 kHz. The time delay, t_{delay} = 0.3032ms.

VIII. CONCLUSION

A Single Phase Matrix Converter (SPMC) operates as Boost Inverter is the new topology that will provide another alternative for application of controlled boost dc-ac inverter operation. The proposed topology could be used for the power factor correction using boost inverter technique for non-linear load operation. The SPMC could be effectively use for controlled boost inverter application. It is shown that the SPMC topology has inherent versatility extending beyond the direct AC-AC converter, DC chopper and rectifier operation. Further advancement could be developed with redundant switches available but are subject to future research. This project describes one such advancement that will be explored. Experience in designing the FPGA for implementation of boost inverter using single-phase matrix converter is has been presented. It has been shown that the FPGA could effectively be used in SPMC with the four bidirectional switching arrangements. SPWM controlling algorithm is placed on a single chip of XC4005XL FPGA and is capable of providing flexibility and design reuse. The overall system is compact with no external memory system required. Tests have been carried out to show the effectiveness and flexibility of the proposed method.

IX. FUTURE RECOMMENDATION

This project can be improved as listed below:

1. Use the suitable capacitor and inductor that acts as a filter to reduce ripple voltage and current which produced from dc supply.
2. Increase the switching frequency of operation to 20 kHz a normal application level associated with the limits of standard IGBT.
3. For further investigation, may include passive filter design to consider good alternative for current source harmonics mitigation. We also can use active filter to modify their compensation characteristic following the dynamic changes of non-linear load.
4. Focus more on inverter operation in induction motor drive application for full investigations.

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