FAULT CURRENT LIMITING USING STATIC SERIES COMPENSATOR

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ABSTRACT

In this paper, a control scheme of the Static Series Compensator (SSC) for fault current limiting has been proposed. The apparatus injects a voltage of variable magnitude in series with a transmission line. This injected voltage is in quadrature with the line current. Under normal condition, it is controlled in order to compensate for reactance of transmission line. When a disturbance occurs, injected voltage from phase shifter is applied to damping control of generator swing. This apparatus is expected to be a promising fault current limiter by using the leakage reactance of series transformer. The proposed methods were applied to 11 busbar system to show its feasibility and capability. All simulation was done using the MATLAB version 7.6 programming.

Keywords:
Static Series Compensator (SSC), fault current limiting, leakage reactance, Flexible AC Transmission System (FACTS).

1.0 INTRODUCTION

The fault current limitation based on impedance control is a quite known subject. Three phase faults can be controlled with limiting reactors and phase-to-ground faults need zero sequence impedance management, sometimes with the use of grounding devices. However, little information exists on short-circuit limitation with series voltage injection, in view of their recent introduction on networks. Since the series voltages are introduced through series coupling transformers, their respective leakage reactance contribute for fault current limitation.

The SSC is a solid-state voltage source and connected in series to power transmission lines in a power system. In this paper, a new control concept for the SSC to contribute to new application referred as fault current limiting has been purposed. Under normal condition, the SSC is controlled to compensate for reactance of transmission line in order to enhance the steady state stability of power system. During a short circuit, maintaining the output voltage from the SSC to be constant equal to the output voltage before the short circuit occur will make the output voltage from the SSC to be insignificant compared with the voltage across leakage reactance of the SSC. Thus, the apparatus is expected to be a promising fault current limiter by setting a certain amount of leakage reactance and the reactance compensation through the SSSC. [1],[2],[3]

The main objective of this project is to reduce the fault current using SSC. Matlab program is used to determine value of fault currents. SSC is place at generator bus because it will give the highest fault current when fault occur.

2.0 STATIC SERIES COMPENSATOR

A SSC operated without an external electric energy sources as a series compensator whose output voltage is in quadrature with, and controllable independently of the line current for the purpose of increasing or decreasing the overall reactive voltage drop across the line and thereby controlling the transmitted electric power. The SSC is based on thyristors without the turn-off capability. A variable reactor such as a Thyristor-Controlled Reactor (TCR) is connected across a series capacitor. When the TCR firing angle is 180 degrees, the reactor becomes nonconducting and the series capacitor has its normal impedance. As the firing angle is advanced from 180 degrees to less than 180 degrees, the capacitive impedance increase. At the other end, when the TCR firing angle is 90 degrees, the reactor becomes fully conducting and the total impedance becomes inductive, because the reactor impedance is design to be much lower than the series capacitor impedance. [1]

2.1 Configuration of the SSC

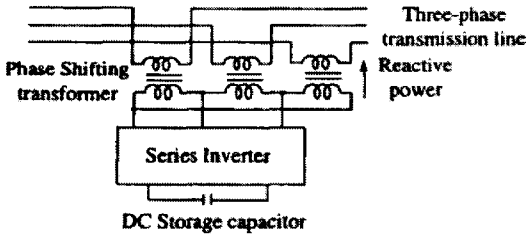


Fig 2.1. Configuration of SSC

The configuration of the SSC is shown in Fig 2. 1. It has a combined structure of phase shifting transformer, a synchronous voltage source (SVS) and dc storage capacitor. The synchronous voltage source can produce a set of alternating voltages approximately sinusoidal at the desired fundamental frequency with controllable amplitude and phase angle. It can therefore generate or absorb reactive power when tied to an electrical power system in the fashion as shown in Fig 2.1. The synchronous voltage source for power transmission applications can be implemented by various kinds of static switching power converters, using semiconductor switching devices of suitable rating and characteristics.

Recent development efforts have focused on voltage-sourced dc to ac inverters, using gate turn-off (GTO) thyristor, in a so-called multipulse circuit configuration. The SVS is connected in series with the transmission line through phase shifting transformer, as shown in Fig 2.1. Figure 2.2 shows a circuit model for power system with the SSC located at generator terminal. The SSC can be modelled as a voltage source connected with the leakage reactance of phase shifting transformer (Xp). Here, Xt is a reactance of a step up transformer and X_l is a reactance of a transmission line.

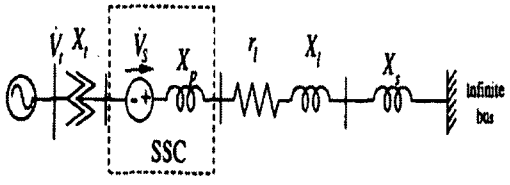


Fig 2.2. Circuit model for power system with the SSC located at generator terminal

An SSC injects an almost sinusoidal voltage, of variable magnitude, in series with a transmission line. This injected voltage is in quadrature with the line current, thereby emulating an inductive or a capacitive reactance in series with the transmission line. This emulated variable reactance, inserted by the injected voltage source, influences the electric power flow in the transmission line.

2.2 Principles Operation of SSC

Simple power system model shown in Fig. 2.3 is used to explain the principle of fault current limiting of the SSC.

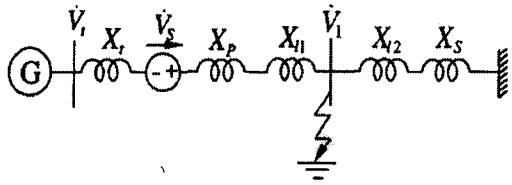


Fig. 2.3. Circuit model used to explain principle of current limiting

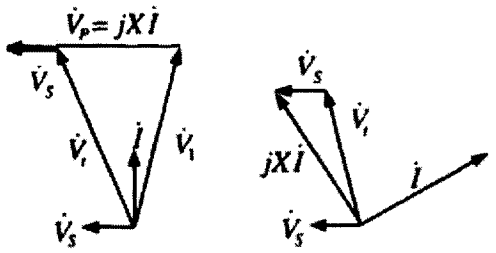
The relation between the current and the voltage under normal condition can be expressed as

$$\dot{V}_t + \dot{V}_s - \dot{V}_1 - jX\dot{I} = 0 \quad \cdots\cdots (1)$$

Here, a reactance of transmission line $X_t=X_{l1}+X_{l2}$. The relation of the vector when V_t and V_1 have a same magnitude in per unit can be expressed in Fig.2.4(a). Phase shifting transformer injects voltage which has phase lagging behind the line current by 90^0 in order to compensate for the reactance of transmission line. When the short circuit fault occur, $V_1= 0$ and the relation between the current and the voltage can be expressed as

$$\dot{V}_t + \dot{V}_s - jX\dot{I} = 0 \quad \cdots\cdots (2)$$

At this time, if voltage injected from the SSC (Vs) is maintained to be constant equal to the injected voltage before the short circuit occur, the vector of the voltage and the current can be expressed as shown in Fig. 2.4(b). It can be seen that the output voltage from the SSC is insignificant compared with the voltage across leakage reactance of the SSC. Therefore, a reactance of phase shifting transformer is contributed to fault current limiting and short circuit fault current is limited by reactance $X=X_p+X_{l1}+X_t$



(a) Normal Condation (b) When fault occur

Fig. 2.4 Control of the SSC

3.0 METHODOLOGY

The aimed of the study is used a SSC as a fault current limiter. In order to reduce the fault current, the SSC is placed at generator bus because the generator bus has the highest fault current. The methods of fault current limiter using SSC are implemented as below.

1. Run the fault program using Matlab programming version 7.6.
2. Analyze the type of fault occur.
3. Inject the voltage from SSC by varying the value of SSC reactance either capacitive or inductive.
4. Check if fault current is reduced.
5. End the program.

The flow chart for the implementation of fault current limiter is shown in figure 3.1.

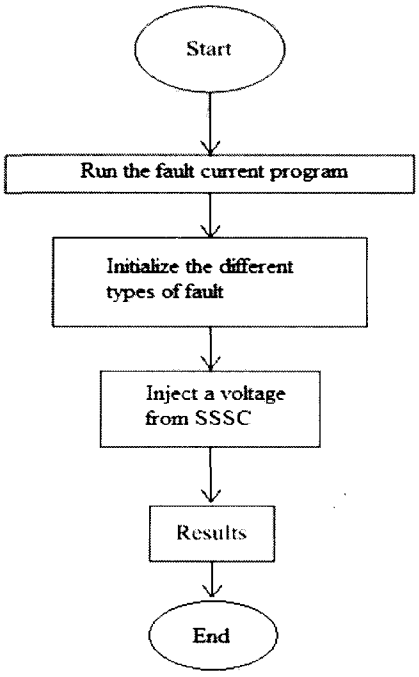


Fig. 3.1 Flowchart for the fault current limiter using SSC

4.0 RESULTS AND DISCUSSION

From the 11 buses system, SSC is placed at the generator bus that is bus 2, bus 10 and bus 11. This three generator bus has the highest fault current when faults occur.

4.1 SSC installed at bus 2

Table 4.1 and 4.2 show the simulation results of the fault current when SSC is installed at bus 2. The value of SSC in table 4.1 is varies from 0 to -1p.u while in table 4.2 the value of SSC is varies from 0 to 1 p.u. Figure 4.1 and 4.2 show the graph for 3 types of fault that is single line to ground, line to line and double line to ground fault.

Figure 4.1 show the highest fault current occurs when SSC is -0.3p.u and the lowest is -0.6p.u for all types of fault. From figure 4.2, the shape of graph shows a reduction for all type of fault.

Table 4.1: Results for fault current after inserting capacitive SSC at bus 2.

Value SSC (pu)	Single line to ground fault (pu)	Line to line fault (pu)	Double line to ground fault (pu)
0	**8.3721**	**5.6989**	**11.504**
-0.1	10.8297	7.7807	13.6289
-0.2	19.0482	16.8018	18.708
-0.3	84.7057	19.2826	46.9459
-0.4	7.5138	3.8179	25.4195
-0.5	2.2355	1.2404	5.0902
-0.6	0.312	0.1791	0.6347
-0.7	0.6839	0.3998	1.3187
-0.8	1.2927	0.7643	2.4156
-0.9	1.7035	1.0149	3.118
-1	1.9993	1.1977	3.6063

Figure 4.1: Graph of fault current Vs value of capacitive SSC at bus 2.

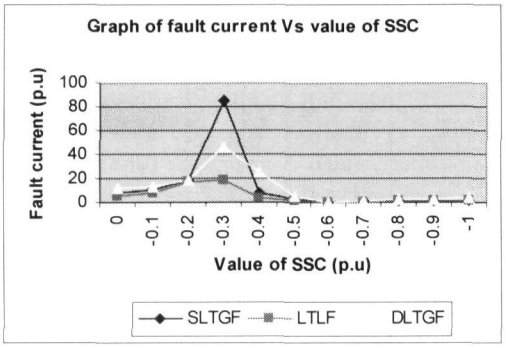
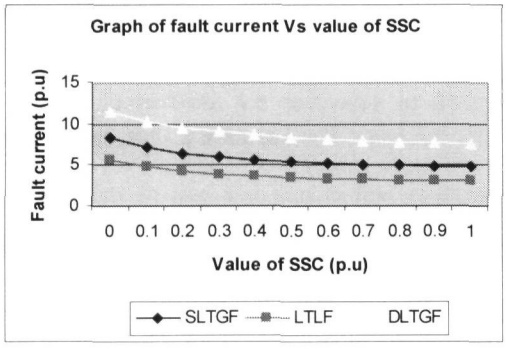


Table 4.2: Result for fault current after inserting inductive SSC at bus 2.

Value SSSC (pu)	Single line to ground fault (pu)	Line to line fault (pu)	Double line to ground fault (pu)
0	**8.3721**	**5.6989**	**11.504**
0.1	7.1901	4.7737	10.3365
0.2	6.4952	4.2507	9.5984
0.3	6.0377	3.9145	9.0895
0.4	5.7138	3.6802	8.7175
0.5	5.4723	3.5075	8.4336
0.6	5.2854	3.375	8.2099
0.7	5.1364	3.2701	8.0291
0.8	5.0149	3.185	7.8798
0.9	4.9139	3.1146	7.7546
1	4.8286	3.0554	7.648

Figure 4.2: Graph of fault current Vs value of inductive SSC at bus 2.



4.2 SSC installed at bus 10

Table 4.3 and 4.4 show the simulation results of the fault current when SSC is installed at bus 10. The value of SSC in table 4.3 is varies from 0 to -1p.u while in table 4.4 the value of SSC is varies from 0 to 1 p.u. Figure 4.3 and 4.4 show the graph for 3 types of fault that is single line to ground, line to line and double line to ground fault.

Figure 4.3 show the highest fault current occurs when SSC is -0.1p.u and the lowest is -0.6p.u for all types of fault. From figure 4.4, the shape of graph shows a reduction for all type of fault.

Table 4.3: Results for fault current after inserting capacitive SSC at bus 10.

Value SSC (pu)	Single line to ground fault (pu)	Line to line fault (pu)	Double line to ground fault (pu)
0	**7.7305**	**7.3204**	**7.1219**
-0.1	17.4295	18.8674	14.5249
-0.2	7.1441	4.2267	13.3234
-0.3	2.9058	1.9173	4.2271
-0.4	1.3892	0.9275	1.9763
-0.5	0.5864	0.3777	0.8947
-0.6	0.0474	0.0277	0.0908
-0.7	0.4639	0.2145	3.6551
-0.8	2.7592	0.3921	0.6741
-0.9	0.2698	0.528	0.1105
-1	0.2439	0.6352	0.1462

Figure 4.3: Graph of fault current Vs value of capacitive SSC at bus 10.

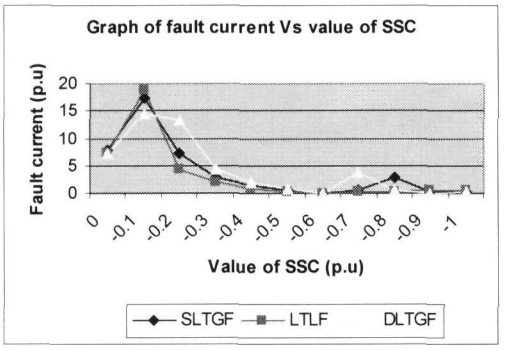


Table 4.4: Result for fault current after inserting inductive SSC at bus 10.

Value SSC (pu)	Single line to ground fault (pu)	Line to line fault (pu)	Double line to ground fault (pu)
0	**7.7305**	**7.3204**	**7.1219**
0.1	5.4099	5.011	5.0796
0.2	4.3672	4.0212	4.1221
0.3	3.7744	3.4714	3.5662
0.4	3.3918	3.1214	3.2029
0.5	3.1243	2.8792	2.9467
0.6	2.9267	2.7016	2.7564
0.7	2.7748	2.5657	2.6094
0.8	2.6543	2.4585	2.4924
0.9	2.5565	2.3716	2.3971
1	2.4754	2.2999	2.3179

Figure 4.4: Graph of fault current Vs value of inductive SSC at bus 10.

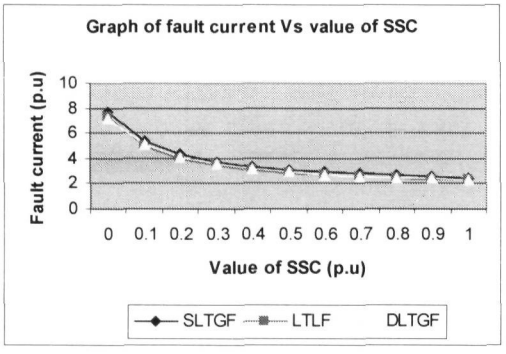
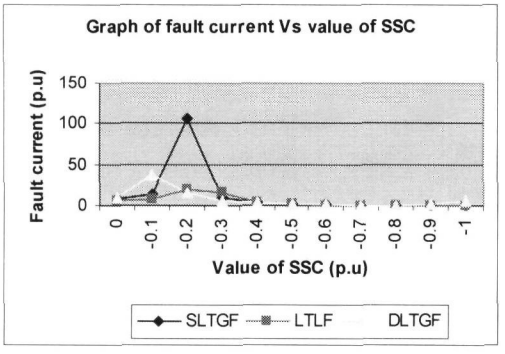


Table 4.5: Results for fault current after inserting capacitive SSC at bus 11.

Value SSC (pu)	Single line to ground fault (pu)	Line to line fault (pu)	Double line to ground fault (pu)
0	**7.0258**	**4.9916**	**8.9956**
-0.1	13.8099	7.301	38.1593
-0.2	106.746	18.848	15.4598
-0.3	9.1	15.793	6.0626
-0.4	4.1213	4.246	3.5547
-0.5	2.2825	1.9366	2.3307
-0.6	1.277	0.9469	1.5348
-0.7	0.6021	0.397	0.8769
-0.8	0.08	0.0471	0.1514
-0.9	0.3724	0.1951	1.0721
-1	0.8051	0.3728	6.2087

Figure 4.5: Graph of fault current Vs value of capacitive SSC at bus 11.



4.3 SSC installed at bus 11

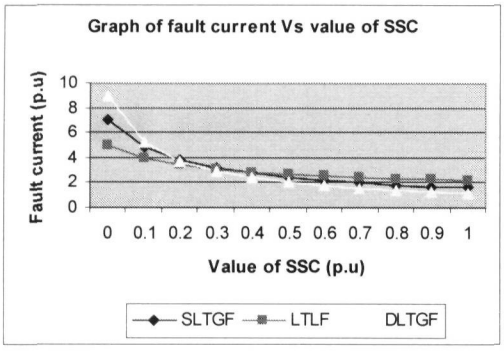
Table 4.5 and 4.6 show the simulation results of the fault current when SSC is installed at bus 11. The value of SSC in table 4.5 is varies from 0 to -1p.u while in table 4.6 the value of SSC is varies from 0 to 1 p.u. Figure 4.5 and 4.6 show the graph for 3 types of fault that is single line to ground, line to line and double line to ground fault.

Figure 4.5 shows the highest fault current occurs when SSC is -0.2p.u for single line to ground and line to line fault. For double line to ground fault, the highest fault current when SSC is -0.1p.u. The lowest fault current occurs when SSC is -0.8p.u for all type of fault. From figure 4.6, the shape of graph shows a reduction for all type of fault.

Table 4.6: Result for fault current after inserting inductive SSC at bus 11.

Value SSC (pu)	Single line to ground fault (pu)	Line to line fault (pu)	Double line to ground fault (pu)
0	**7.0258**	**4.9916**	**8.9956**
0.1	4.8954	4.0018	5.2047
0.2	3.8375	3.452	3.6997
0.3	3.1971	3.1021	2.8869
0.4	2.7633	2.8598	2.3756
0.5	2.4475	2.6822	2.0231
0.6	2.2055	2.5463	1.7646
0.7	2.0133	2.4391	1.5665
0.8	1.8561	2.3523	1.4097
0.9	1.7246	2.2805	1.2822
1	1.6128	2.2203	1.1764

Figure 4.6: Graph of fault current Vs value of inductive SSC at bus 11.



5.0 CONCLUSION

This project demonstrates the performance of SSC as a fault current limiter. The SSC can operate either inductive or capacitive. The results show that the most effective way for SSC to reduce the fault current is operate as capacitive. When the SSC operate as capacitive, it can reduce the fault current until 1.0p.u and above. When a fault occurs, maintaining the output voltage from the SSC to be constant equal to the output voltage before the short circuit occur is considered to be an effective way to apply for limiting the fault current. As a result the apparatus with the proposed control scheme is considered to be a promising fault current limiter.

6.0 FUTURE DEVELOPMENT

This project on reducing fault current by SSC can be continued by power system stabilization. The injected voltage from the SSC is in quadrature with the line current and it affects the phase angle between the sending-end and receiving-end voltages, therefore the SSC is capable of controlling the power flow through the alternating current transmission line by injecting an appropriate output voltage. Here, in order to increase the damping of power swing, the output voltage from the SSC is generated by using the generator angular velocity as a feedback control signal. The power system stabilization can be model using MATLAB Simulink.

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