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A 93.36 dB, 161 MHz CMOS Operational Transconductance Amplifier (OTA) for a 16 Bit Pipeline Analog-to-Digital Converter (ADC)

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ABSTRACT

A gain modified CMOS Operational Transconductance Amplifier (OTA) for a 16 bit pipeline Analog-to-Digital Converter (ADC) is presented. The circuit is designed to be used for a high resolution and low sampling rate ADC. Gain boosting technique is implemented in the design to achieve high DC gain and settling time as required. Post layout simulations for a 5 pF load capacitance shows that OTA achieves a gain bandwidth of 161 MHz at a phase margin 93.14^{o} with 93.27 dB DC gain. The settling time for an OTA is 163 ns for 0.1 % accuracy to achieve final value and consume power about 4.88 mW from 5 V power supply.

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1. INTRODUCTION

In high performance analog integrated circuits, such as a pipeline A/D converters, operational amplifier (Op Amp) with very high DC gain and high unity gain frequency are needed to meet both accuracy and fast settling requirements of the systems. However, as a CMOS design scales into low power, low voltage and short channel CMOS process regime, satisfying both of these aspects leads to contradictory demands, and becomes more difficult since the intrinsic gain of the devices is limited. As the CMOS devices are sized for large transconductance to achieve high gain bandwidth (GBW) and high DC gain for fast and accurate settling time, the attendant parasitic capacitances severely erode the amplifier phase margin (PM), thus reducing GBW [1],[2], [4],[5]. Hence, a single stage gain enhanced OTA topology that approximates a single pole system was considered ideal for the above low voltage requirements.

A gain boosting technique is included that increases the gain of a normal cascode stage without affecting the frequency behaviour to a large extent. A number of work has been reported with [1] achieving 870 MHz GBW and 92 dB DC gain at 1.5 V uses 0.35 µm CMOS process. A DC gain of 129 dB and about 161 MHz GBW was achieved in [3] for a 0.35 µm CMOS design but with a 3.3 V operating voltage. The OTA design reported in [7] achieves 105 dB DC gain and 90 MHz GBW at a 3.3 V but consumes 4.8 Mw. Based on the previous work, it is well known that active cascode gain boosting technique can be used to increase the DC gain of an operational amplifier without degrading its high frequency performance.

2. CIRCUIT IMPLEMENTATION

This section describe research chronical including circuit design process, how to determine the current and gain for the main amplifier architecture and test the performance parameter.

2.1. Main Amplifier Design

The operational amplifier will be used in a data converter with a resolution of 16 bits and it must amplify signals to within ½ least significant bits (LSB) of the ideal value [8],[9],[10].The closed loop gain of an amplifier can be determined by this equation;

$$A_{CL} = \frac{A_{OL}(f)}{1+\beta.A_{OL}(f)} \tag{1}$$

The output of the amplifier will be equal to its ideal value minus some maximum deviations, ΔA. The gain of the DAI over one clock cycle is

$$\left| A_{CL} = \frac{C_I}{C_F} \right| \tag{2}$$

The minimum required DC open loop gain can be estimated as

$$\left|A_{OLDC}\right| \geq \frac{1}{\beta}.2^{N+1} \tag{3}$$

By assuming $\beta = 1/2$ and $C_I = C_F$ this equation can be reduced to

$$\left|A_{OLDC}\right| \geq 2^{N+1} \tag{4}$$

The 16 bit converter must have $\left|A_{OLDC}\right| \geq 262144$ or 108 dB. The speed of a data converter is mainly limited by the Op Amp used. The minimum Op Amp gain bandwidth product (f_u) required for a specific settling time t (where t is less than $1/f_{clk}$, within a dead band of $\pm 1/2.LSB$) can be estimated by this equation;

$$V_{out} = V_{outfinal}\left(1-\frac{1}{2^{N+1}}\right) = V_{outfinal}\left(1-e^{-t/\tau}\right) \tag{5}$$

$$\tau = \frac{1}{2\pi.\beta.f_u} \tag{6}$$

The minimum required Op Amp unity gain frequency is given by

$$f_u = \frac{f_{clk}.\ln 2^{N+1}}{2\pi.\beta} \tag{7}$$

By assuming $\beta = 1/2$

$$f_u \geq 0.22(N+1).f_{CLK} \tag{8}$$

For a 16 bit pipelined ADC that is clocked at 1 MHz, the required Op Amp must have unity gain frequency, f_u at 3.74 MHz (and at least a dc gain of 108 dB).

Since the OTA is to be used in the multiplying digital analog converter (MDAC) of a 1 MS/s, 16-bit pipeline ADC design, it requires that the output to settle to 0.1 % in ¼ the period (250 ns). The desired ADC input range is 1 V_{P-P} differential. For a step input, the output of a first system is given by:

$$V_O(t) = A\left(1 - e^{-t/\tau}\right) \tag{9}$$

where τ is the time-constant and *A* is the final amplitude which in this case is 1 V.

Thus, for 0.1 % accuracy, the settling time is about 8τ. An additional 1τ is added for slewing bringing the total to 9τ. The slew rate (SR) of OTA can be determined using this equation. It shows that the OTA must be able to slew at 36 V/μs.

$$SR = \frac{V_O}{\tau} = 36V/\mu s \tag{10}$$

By choosing the load capacitor of 2 pF, the required current that is used to charge (or discharge) each load capacitor must be 180 μA in order to meet the slew rate specification.

2.2. OTA Topology

Single stage Op Amp is suitable for high gain design because it has good bandwidth without any compensation. A fully differential folded cascode Op Amp that has 4 single ended OTA has been chosen. In order to achieve high gain and speed, the Op Amp employ NMOS input differential pair. The complete implementation is shown in Fig. 1. This design incorporates fully differential inputs, outputs, a folded cascode bias circuitry with common mode feed back and gain boosting amplifiers. The OTA can be divided into four parts: the bias circuit, the amplifier circuit, the common mode feedback circuit and the gain boosting circuit.

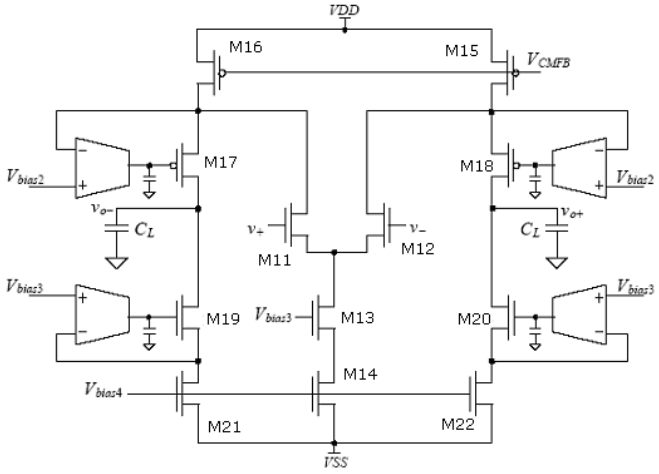

Figure 1. Fully differential folded cascode Op Amp with gain boosting amplifiers

Fully differential folded cascode Op Amp is shown in Fig. 2. A differential pair is used to sense the input voltage difference. If the pair is operating in saturation, when one transistor is turned on, the other will turn off. The current through one leg will be sourced to the output while the other leg will sink current from the load. The input transistors were sized with a very large W/L ratio to provide the high transconductance required to quickly move charge onto the test capacitors. Special care must be taken to ensure that the input differential pair is operating in saturation and not in the triode region. Operation in the triode region will cause the behavior of the OTA to be nonlinear and will result in poor transient response as well as a loss in dc gain.

Gain enhancement technique is used to increase the gain of an Op Amp. In this project, single ended Op Amp has been used as a gain boosting amplifier. It has been implemented in the main amplifier circuit as shown in the Fig. 3. The idea of gain boosting technique is based on negative feedback loop to set the drain of voltage M21. Negative feedback drives the gate of M19 until V_x has the same value as V_{bias3}. Therefore, the variation of V_{out} has much less effect on V_x because the boosting Op Amp A_{OTA} regulated this voltage [3]. Thus, the output impedance of the circuit is increased by the gain of the additional gain stage A_{OTA}, as shown in the following equation;

$$R_{OUT} = (g_{m19} r_{o19} (A_{OTA} + 1) + 1) \times r_{o21} + r_{o19} \quad (11)$$

$$\approx A_{OTA} g_{m19} r_{o21} r_{o19} \quad (12)$$

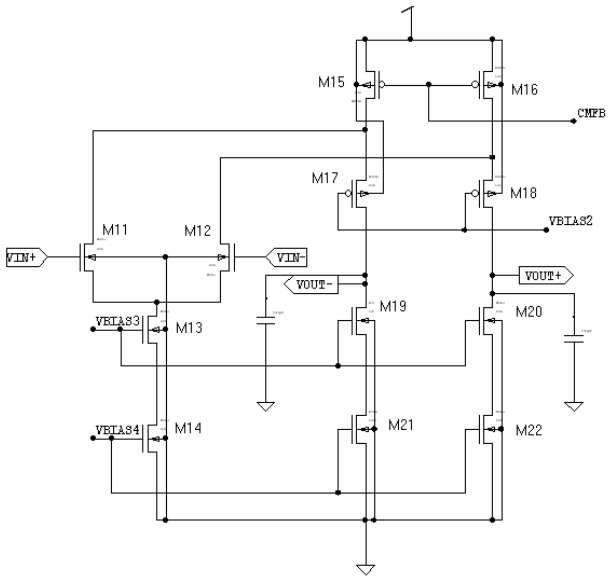

Figure 2. Fully differential folded cascode Op Amp

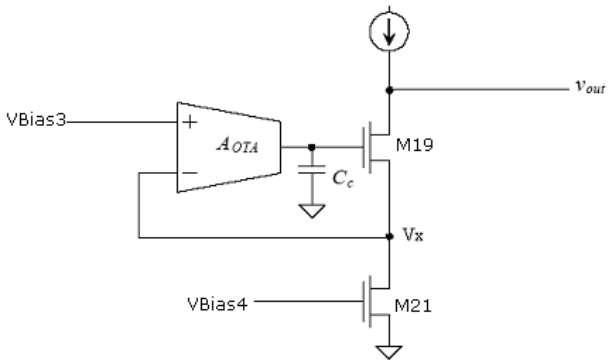

Figure 3. Gain enhancement to increase cascode open circuit gain

Both the dc gain and the output impedance of the main Op Amp are multiplied by a factor of about (1 + A_{OTA}), where A_{OTA} is the gain of the additional feedback path. According to the output impedances, the overall dc gain can be increased several orders of magnitude, as shown in the following equation;

$$A_{TOTAL} = g_{m21} R_{OUT} = A_{OTA} g_{m21} g_{m19} r_{o21} r_{o19} \quad (13)$$

3. RESULTS AND DISCUSSION

Simulation of both schematic and layout of the OTA was done using TANNER EDA Tool. The Op Amp has been implemented in 0.5 µm CMOS14TB process with 5 V power supply. The AC simulation results are shown in Fig.4. It shows that the dc gain is 93.36 dB and the bandwidth is 161 MHz. The phase margin is about 93^0.

With a unity gain configuration, the slew rate and settling time are measured. The transient response of the test circuit is shown in Fig. 5. The plot on the top of the figure shows the input and output of the OTA while the plot in on the bottom shows the differential output voltage. The goal is to achieve a difference of 1

V after settling between the outputs, with at least 16 bits accuracy. Fig. 5 shows a typical settling time measurement. The differential output settles to 999 mV in 163 ns, and back down to less than 1 mV in 163 ns.

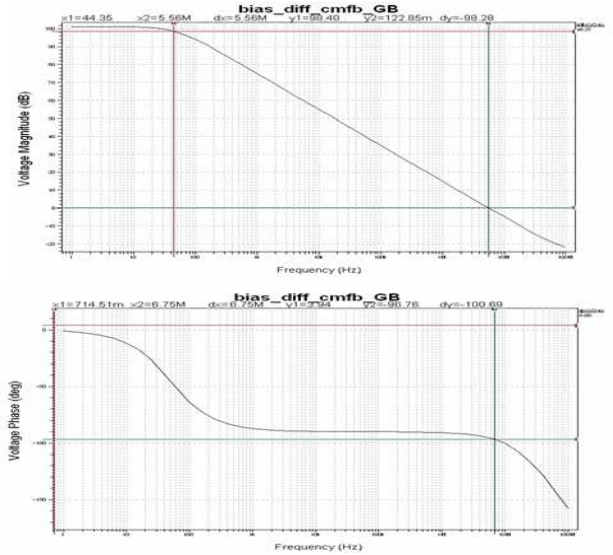

Figure 4. AC response of Op Amp

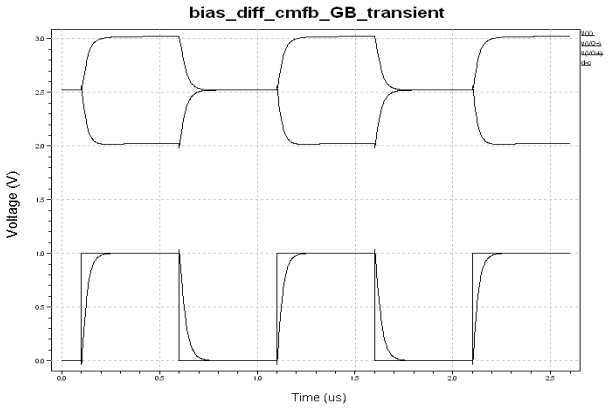

Figure 5. Simulated transient response of Op Amp

The main characteristics of the Op Amp are summarized in Table 1. The results shows that the gain boosted technique improve efficiently the dc gain without affecting the speed of Op Amp.

Table 1. Post-layout amplifier performance summary

Parameter	Value
Technology	0.5 um CMOS14TB
DC Gain without gain boosting	48.8 dB
DC Gain with gain boosting	93.36 dB
Phase Margin	93.14 ^{o}
Bandwidth	161 MHz
Slew Rate	36 V/µs
Output voltage swing	1.75 – 4.86 V
Settling time (0.1%) accurate	163 ns
Supply Voltage	5 V
Power Dissipation	4.88 mW
Load Capacitor	5 pF
Area	0.089 mm^2

4. CONCLUSION

The design of a single stage fully differential operational amplifier with gain boosting amplifier for 0.5 µm CMOS14TB is presented in this paper. With the load capacitor of 5 pF, the design demonstrates a dc gain of 93.27 dB with a bandwidth of 161 MHz and phase margin of 93.14 ^{o}. This design is tailored for high resolution with low sampling rate pipelined ADC and it will be used in a 16 bit pipelined ADC.

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