NBTI Effects on Circuit Reliability Performance of 4-bit Johnson Counter Based on Different Simulation Configuration

M. F. Zainudin, H. Hussin, J. Karim, and A. K. Halim

***Abstract*— Negative-bias temperature instability (NBTI) has become a serious circuit reliability concern as technology nodes decrease to nanometer scales. This paper presents comprehensive analyses of the NBTI effect on 4-bit Johnson Counter with a 16-nm High Performance (HP) Predictive Technology Model (PTM). The threshold voltage shift and delay degradation of Johnson Counter are analyzed in the presence of NBTI degradation using a MOSRA model based on different configuration of stress measurement with different diffusion species. The threshold voltage shift for the simulation with no circuit cut-off time is higher than the simulation with circuit cut-off time. Not only that, threshold voltage shift with atomic hydrogen species also shows the highest compared to molecular hydrogen species. As a result, simulations with no circuit cut-off time with atomic hydrogen species contribute the highest NBTI degradation. The results show that the main concern of NBTI degradation impact on the circuit performance can increase the delay up to 15.31% and an average power reduction of up to 13.31% in 10-year lifetime.**

***Index Terms*— Negative-bias temperature instability (NBTI), performance, reliability, dynamic NBTI**

I. INTRODUCTION

JOHNSON COUNTER is widely used as a decade frequency divider and multiphase clock signal generator. It can produce glitch free symmetric (50% duty cycle) outputs per count cycle and can also be used to drive stepper motor circuits [1], [2]. Fig. 1 shows a 4-bit Johnson Counter with terminal count output, *tc*. At the same time, Negative-bias Temperature Instability (NBTI) has long been a critical reliability problem for a scaled pMOS transistor. NBTI results in a sudden changes of threshold voltage shift (ΔV_{TH}) [2]-[3] which later affects the circuit performance [5]–[7]. NBTI now become an important reliability issues with the introduction of FinFET technology and high-k metal-gate technology, especially beyond 16-nm nodes, according to 2015 International Technology Roadmap for Semiconductors (ITRS) reports.

To date, research works on NBTI are currently active within the community due to the progressive technology node scaling down to 16-nm node. To the best of our knowledge, studies on NBTI focus on the device and reliability physics. This is due to the lack CAD tools with NBTI model degradation are not widely available. CAD tools like Synopsys HSPICE introduced MOSFET Reliability Analysis (MOSRA) [8] together with the NBTI model in order to handle this problem by predicting NBTI degradation. Predictive Technology Model (PTM) [9] are currently used as a cornerstone of circuit design and optimization with the presence of NBTI degradation [8–10].

In this work, a simulation framework to predict the NBTI effect on circuit reliability performance based on the different Hspice reliability simulation is presented. The evaluation of NBTI degradation will be measured according to the ΔV_{TH} value. Then, an investigation on the relationship of the NBTI degradation and the circuit performance based on delay time and power consumption will be analyzed and discussed.

The remainder of the paper is organized as follows. In Section II, details of our MOSRA simulation with the presence of NBTI model used in conjunction with 16-nm High Performance Predictive Technology Model (PTM) are described. The effects of NBTI degradation on the delay time and power consumption of the terminal count logic gates of Johnson counter are explained in Section III. Finally, the conclusion is presented in Section IV.

II. SIMULATION METHODOLOGY

A. Circuit under Test

The 4-bit Johnson Counter with terminal count output, *tc* as shown in Fig. 1 will be simulated using Synopsys HSPICE. This counter will be simulated with the presence of the NBTI model provided by MOSRA based on 16-nm High Performance PTM. PTM is a virtual model card usually used in simulation work since the parameters in PTM is verified with the actual conventional silicon planar MOSFET device scaling according to the International Technology Roadmap for Semiconductors (ITRS) [13].

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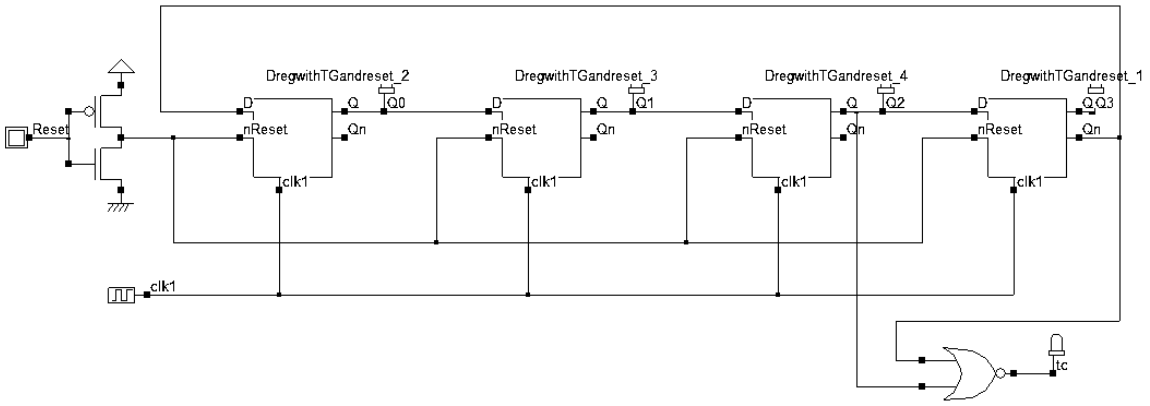


Fig. 1.Schematic for 4-bit Johnson Counter with terminal count circuit.

In this work, the D Flip-Flop used for the Johnson Counter is shown in Fig. 2. NBTI degradation is measured based on the changes of the threshold voltage, ΔV_{TH} at the pMOS transistor logics at the terminal count (tc) output. The delay measurement is measured based on the clock input to terminal count output (T_{CtoTc}), whereas the power measurement is measured based on the average power reported in the Synopsys's HSPICE output file. These characterized performance data has been implemented from previous work of [14] and [15] where focuses on the flip-flop characterized data performance.

In this work, the Device under Test (DUT) is simulated at a temperature of 125°C and the nominal voltage input of 0.7V for 10 years of stress time with the stress voltage considered as DC. The temperature and the nominal voltage are set based on previous work related to NBTI condition where the range for temperature study is between 25°C to 125°C [16] and the range for voltage supply study is between -0.5% to +1.5% [17]. Since the work focuses on were simulation setup configuration and hydrogen diffusion species, the value is set according to the range of temperature and voltage supply based NBTI condition.

The parameters chosen to be varied were simulation setup configuration and hydrogen diffusion species. The simulation step configurations vary based on the percentages of stress time and circuit cut-off time in a period of 1 sec. The threshold voltage shift is observed to be different based on different simulation stress time in [18]. Different stress and recovery time gives different value of threshold voltage shift and this work motivates the author to apply this technique to observe its effect on the circuit performance parameters.

The hydrogen diffusion species considered in this work are atomic hydrogen (H) and molecular hydrogen (H_2) with the power-law time exponent, $n = 1/4$ and $n = 1/6$ respectively [19]. The power-law exponent is observed to be different when the circuit undergo different stress time and recovery time. Normally if the circuit only focuses on stress without recovery time, the power-law time exponent is observed to be $n \sim 0.25$. Meanwhile, the power-law time exponent seem to be different when the circuit is given a recovery time which is in range $n \sim 0.167$.

The threshold voltage shift, delay time, and average power measurement are measured for each of 1/10 (post-stress reported per year) of the total stress time (10 years lifetime). The characterized data used is similar with the previous data [5] that focuses on the domino circuit performance.

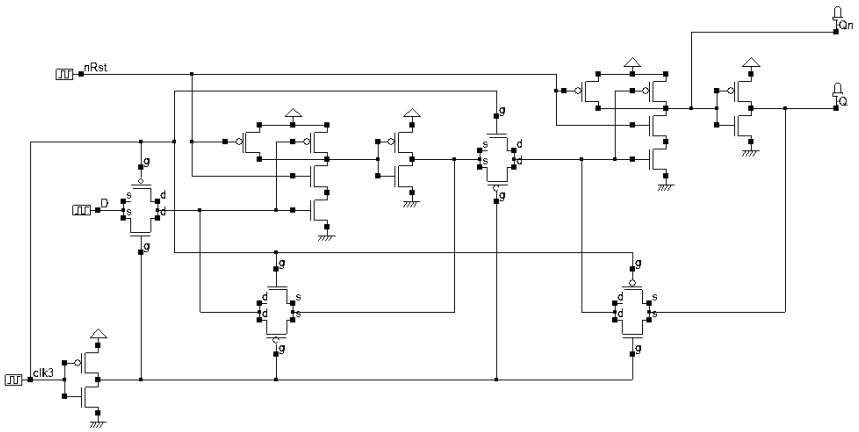


Fig. 2.Schematic for D Flip-Flop with Transmission Gate with nReset.

B. *HSPICE Reliability Simulation Commands by MOSRA*

Use Three different HSPICE reliability simulation configuration as shown in Fig. 3 were used in order to understand the impact of NBTI degradation to circuit performance based delay time and average power. The value of post-stress simulation of ΔV_{TH} is reported in (.radeg) output file while the circuit delay time and average power in (.mt) output file [8]. The delay times were calculated from the average of the delay input from the low transition to the high transition (t_{PLH}) and the delay input from the high transition to the lower transition (t_{PHL}).

The format for the HSPICE reliability simulation is as follows: First, the circuit was under stressed under a transient time which starts at 0.1ns and ends at 40ns. Next, the simulation will continue to be stressed until it achieves the total stress time (10 years). The first simulation was considered to be 100% stress time with no circuit cut-off time.

Second, the simulation was considered to be under 1% stress time and 99% circuit cut-off time. The circuit experiences the aging effect starting from 1ns until it stops at 40ns. Later, the circuit is under no stress from 40ns until 1s. Then, for aging period of 1, the simulation continues to be stressed until it reaches the total stress time.

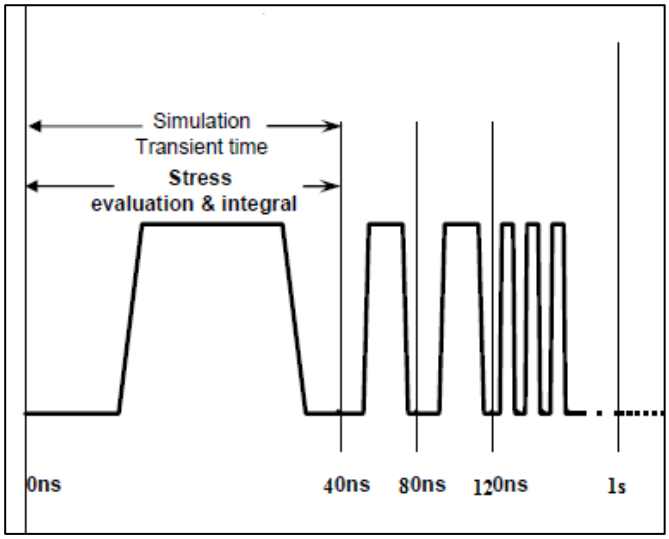
Last, the simulation was similar to the first simulation configuration. However, the circuit is simulated from 0.1ns until the aging width of 0.5s and later the circuit will be under cut-off time from 0.5s until 1s. The third simulation configuration was considered to be under 50% stress time and 50% cut-off time.

The goal was to study how these simulation configurations would affect the NBTI degradation based on the changes of threshold voltage. Later, the circuit performance can be related with ΔV_{TH} to understand how NBTI degradation affect the circuit performance under a long aging period.

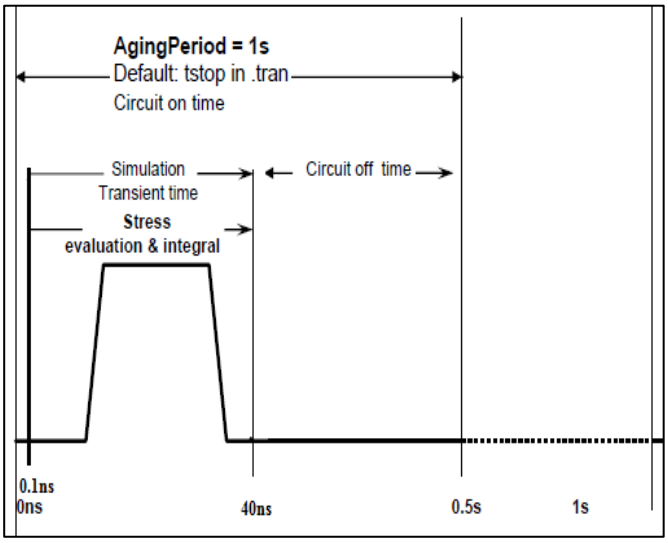
In Reaction-Diffusion (R-D) model, there are two components that contribute to the ΔV_{TH} based on the pre-existing interface traps and the new interface traps generation [20]. The first component was classified as Permanent (Non-Recoverable) which was the same as the first simulation configuration. Permanent NBTI is due to the new interface trap generation as a result of the broken bond of Si-H. The ΔV_{TH} is permanent as the stress continues.

The other component was Temporary (Recoverable) which were similar to the second and the third simulation configuration. It was known as temporary because ΔV_{TH} was recovered when the stress voltage was removed. The interface traps can be removed due to pre-existing traps located at the silicon-oxide interface was filled with holes from the channel of pMOS [20]. The interface traps later recombine back with H atom into a Si-H bond.

Based on the simulation configuration, the second simulation was expected to produce the least ΔV_{TH} between the other two simulations due to the longer cut-off time. The first simulation will contribute to the highest ΔV_{TH} due to the longer stress time. The results for this experiment are shown in Section III.



(a)



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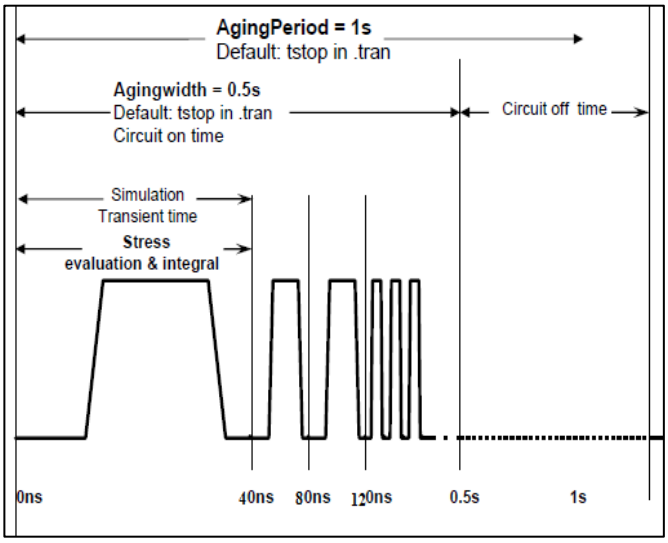

(c)

Fig. 3.Graphic Illustration of MOSRA Command (a) 100% stress time (b) 1% stress time and 99% cut-off time (c) 50% stress time and cut-off time.

III. SIMULATION RESULT AND DISCUSSION

In this section, the simulation results of the NBTI degradation based on three different HSPICE reliability simulations is presented. First, the diffusion species based on atomic hydrogen (n = 1/4) were tested to investigate the NBTI degradation based on the permanent component. Then, the diffusion species of molecular hydrogen (n = 1/6) was used to examine the NBTI degradation with the presence of the recoverable component. The simulation outputs were obtained from the output reports of (.radeg) and (.mt) output files format after post-stress simulation.

A. Effects of Different Simulation Configuration on Threshold Voltage Shift

The overall ΔV_{TH} after 10 years for the first, second, and third simulation configuration were 19.282mV, 0.277mV, and 16.254mV respectively. The percentages of ΔV_{TH} were calculated and the percentage for the first, second, and third simulation were increase up to 7.55%, 8.12% and 7.5% respectively. Although the second simulation has the highest ΔV_{TH} percentage, the actual values were actually too small and had the least effect on the circuit performances.

The ΔV_{TH} for Johnson Counter were observed and the first simulation configuration exhibits larger ΔV_{TH} as shown in Fig. 4. Same observation reported in [3], where the first simulation configuration produce larger ΔV_{TH} due to the fact of interface traps generation. Since there was no cut-off time, new creation of interface traps (N_{IT}) gradually build up during stress due to the broken bonds of Si-H in the interface [3]. These interface traps (the dangling incomplete bond of Si) from the broken Si-H bond are responsible for the temporal shift of the threshold voltage [4]. Thus, higher interface trap generation causes higher changes in threshold voltage.

However, the ΔV_{TH} for second simulation configuration were the lowest between the first and third simulation configuration. This was because the second simulation configuration had the shortest stress time (1%) and interface traps slowly built up during the stress time and stopped during the circuit cut-off time. Since the diffusion species was based on the atomic hydrogen (n = 1/4), the interface traps become a permanent NBTI component without the presence of the oxide trap (N_{OT}) for the ΔV_{TH} to recover during the cut-off time.

Next, the changes in threshold voltage were observed based on molecular hydrogen (n=1/6). Fig. 5 shown the difference of ΔV_{TH} between the atomic hydrogen and molecular hydrogen. Per Fig. 5, ΔV_{TH} based on the atomic hydrogen diffusion species is higher than the molecular hydrogen diffusion species. This observation was different from what was reported in [19] in which the ΔV_{TH} for the atomic hydrogen (n =1/4) was less than molecular hydrogen (n = 1/6). The molecular hydrogen contributes to lower NBTI degradation due to ΔV_{TH} being recovered over time during the circuit cut-off time in the presence of oxide trap (N_{OT}) [3]. These traps are located in the bulk of the dielectric and were filled by holes during the stress and evaluation phase. Later, these traps can be emptied after the stress voltage was removed. Thus, the threshold voltage is recovered during the recovery time and result in lower threshold voltage shift compared to observation based on molecular hydrogen effect.

B. Effects of NBTI Degradation on Delay Time

The percentage of delay change due to NBTI degradation during a circuit lifetime of 10 years is shown in Fig. 6. The delay time were measured from clock input to terminal count output based on t_{PLH} and t_{PHL}. Then, the propagation delay, t_D was calculated based on the average value of the t_{PLH} and t_{PHL}. As shown in Fig. 5, the second simulation had almost no impact on the circuit delay for both diffusion species where the delay was the same value with 0.002% increment on the circuit delay time. This was due to the fact that the ΔV_{TH} was too small compared to the other two simulations.

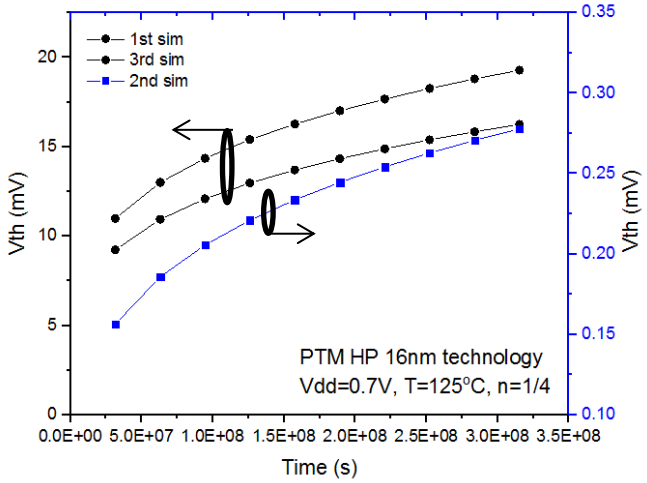

Fig. 4.The threshold voltage shift based on different HSPICE reliability simulation commands.

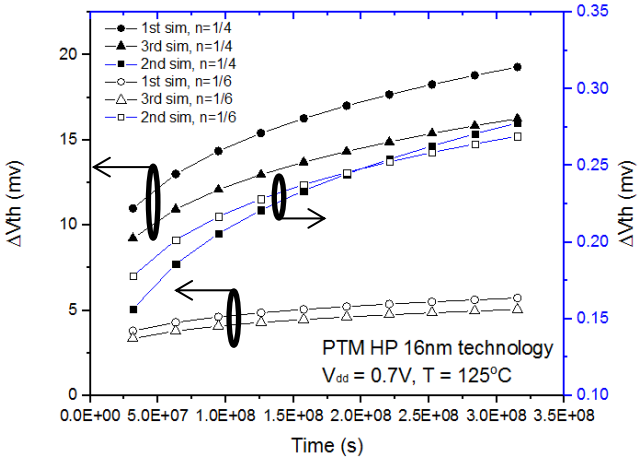

Fig. 5. The shift of the threshold voltage based on different diffusion species.

The degradation impact on delay can also be described considering from the previous gate delay model where the delay degradation Δt_{pd} for the gate was derived as [21] with the Taylor series expansion:

$$\Delta t_{PD} = \frac{\alpha \Delta V_{TH}}{V_{GS} - V_{TH0}} \bullet t_{PD0} \tag{1}$$

where α is the velocity saturation index. The Δt_{pd} is proportional to ΔV_{TH} which leads circuit delay time to increase when the ΔV_{TH} increase. As it can be seen in Fig. 6, the NBTI degradation causes an increase of more than 0.265% (first simulation) and 0.203% (third simulation) in the circuit delay time during a lifetime of 10 years based on the atomic hydrogen diffusion species. This observation was in agreement with [5], [22], [23] where the circuit delay increases due to NBTI degradation. Theoretically, the delay increases because the terminal output transition speed decreases. Not only that, a slower transition in the output from the inverter pMOS transistors in the output of 4-bit Johnson Counter turns on/off later, which in turn leads to more contention and a slower transition [5] for each D Flip-Flop stage and consequently a slower transition of the terminal output.

Based on the observations from Fig. 6, the output signal is seen to shift from fresh to 10 years of circuit lifetime. In HSPICE, the delay time has been calculated based on the average of the t_{PLH} (delay input from 50% to output when the output is rising) and t_{PHL} (delay input from 50% to output when the output is falling) [24]. Based on the graph obtained using Synopsys Cscope, the delay time was observed to shift mainly during the rising time (t_{PLH}).

Equations 2 and 3 shows the delay shift during the rising time (t_{PLH}) and the falling time (t_{PHL}) of the reference output at the terminal count. From the equation below, t_{PLH} increases as the ΔV_{TH} because ΔV_{TH} is proportional to t_{PLH} as proven from [25]:

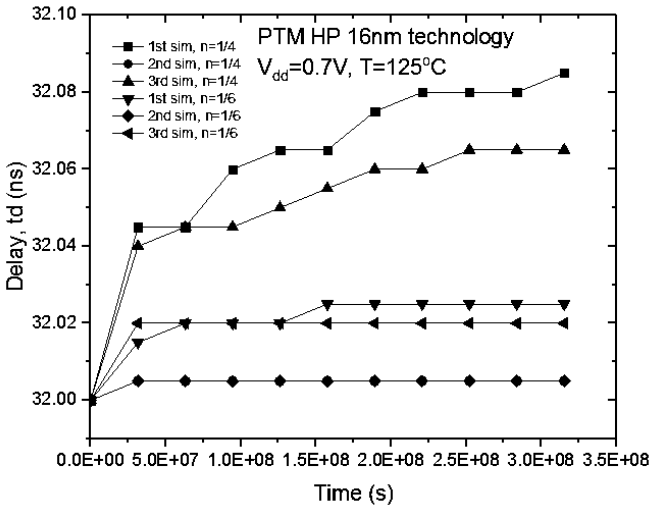

Fig. 6. The percentage of delay shift based on different HSPICE reliability simulation.

$$t_{PLH} = \frac{C_L}{K_{P'}(V_{DD} - |V_{TH,P}|)} \bullet \left[\frac{2 \bullet |V_{TH,P}|}{(V_{DD} - |V_{TH,P}|)} + \ln\left(\frac{4\left((V_{DD} - |V_{TH,P}|\right)}{V_{DD}} - 1 \right) \right] \tag{2}$$

$$t_{PHL} = \frac{C_L}{K_{P'}(V_{DD} - |V_{TH,N}|)} \bullet \left[\frac{2 \bullet |V_{TH,N}|}{(V_{DD} - |V_{TH,N}|)} + \ln\left(\frac{4\left((V_{DD} - |V_{TH,N}|\right)}{V_{DD}} - 1 \right) \right] \tag{3}$$

The equations show that t_{PLH} increased due to NBTI degradation on p-MOSFET transistoros while t_{PHL} remained unchanged after 10 years since NBTI does not degrade n-MOSFET transistors electrical properties. During the stress period, the nMOS transistor is cut-off and the pMOS transistor is supplied by saturation current (I_{DPSAT}) to charge up the gate and parasitic capacitances. NBTI degradation caused an increase of ΔV_{TH} in pMOS transistor [3]. Meanwhile, the falling time (t_{PHL}) remains unchanged as the terminal count was supplied by nMOS saturation current ($I_{Dn(SAT)}$) and the pMOS transistor was cut off. Since the NBTI degradation only involves the pMOS transistor, t_{PHL} was not affected by NBTI degradation.

C. Effects of NBTI Degradation on Power Consumption

Fig. 7 shows the effects of NBTI degradation on average power. The average power is observed to have decreased as the stress time increased. Over 10 years of stress time, the first simulation has the highest average power reduction at 15.31% from fresh to 10 years based on the atomic hydrogen diffusion species. Meanwhile, the second simulation produced the lowest ΔV_{TH} with an average power reduced only up to 0.23% which was the same for both diffusion species. This is due to the fact that average power has a relationship with ΔV_{TH}. The average power in SPICE can be described as:

$$P_{Tavg} = \frac{1}{T}\int_0^T \left[P_{Dynamic} + P_{Static} + P_{Leakage} \right] dt \tag{4}$$

$$P_{Leakage} = V_{DD} \bullet I_{Peak}\left(\frac{t_{Rise} + t_{Fall}}{2} \right) \tag{5}$$

where T is the period of interest, and I_{peak} is the peak or maximum transient current when the output node voltage rises from V_T to $V_{DD} - V_T$ or falls from $V_{DD} - V_T$ to V_T [25]. The ratio of rising time, t_{rise} and fall time, t_{fall} can be expressed as follows:

$$\frac{t_{Rise}}{t_{Fall}} = \frac{I_{DnMax}}{I_{DpMax}} = \frac{\mu_n}{\mu_p}\left[\frac{W_{NMOS} \bullet (V_{DD} - V_{THN})}{W_{PMOS} \bullet (V_{DD} - V_{THP})} \right]^2 \tag{6}$$

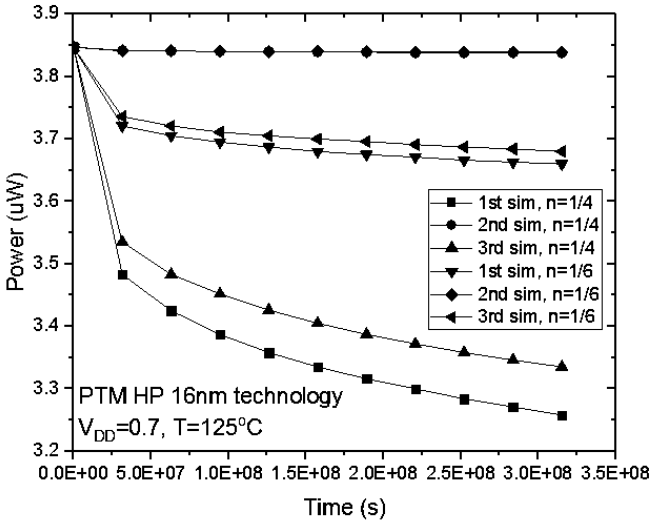

Fig. 7. The changes of average power from fresh to 10 years simulation.

The ratio in (6) clearly shown that t_{rise} depend on the nMOS transistor while t_{fall} is depend on the pMOS transistor. The subthreshold leakage power (I_{Dpmax}) decrease due to the increasing of V_{THP} which later result in a reduction of $P_{leakage}$ [5]. The increasing of ΔV_{TH} from the 4-bit Johnson Counter makes the output transition slower which later increase the contention power of the Johnson Counter. As a result, the contention power of the terminal count output decreases. Not only that, the on-state current for all the circuit device is also reduced which later affect the average power. The threshold voltage shift for the simulation with no circuit off-time was the highest compared to the longest cut-off time.

IV. CONCLUSION

This paper presents a simulation framework analyzing the impacts of NBTI on the circuit performance of terminal count logic gates in a 4-bit Johnson Counter based on PTM 16-nm High Performance technology models. The results have shown that due to the NBTI-induced degradations, the ΔV_{TH} of the first simulation higher than the other two simulations. Not only that, the diffusion species based on the atomic hydrogen was shown to have the more dominant NBTI degradation over the molecular hydrogen. The circuit delay time increased for the 10 years of circuit lifetime up to 0.266% for the first simulation while the average power reduces up to 15.31% based from observation from simulation with no circuit cut-off time. Based on observation on Synopsys CSCOPE, changes in circuit delay time were observed and t_{PHL} was found to be the main factor contributing to the circuit delay shift. We have shown that different simulation configurations could give different NBTI degradation patterns. Not only that, circuit performance was also observed in the presence of NBTI degradation.

V. ACKNOWLEDGMENT

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