Tunable High Speed Pulse Generator for Phase Change Memory(PCM)

R. I. Alip, T. N. T. Yaakub, M. Rasin, M Fazullah, H. Hazwan

***Abstract*—This project presents a model representation of storing data in a Phase Change Memory (PCM) using a high speed pulse generator. PCM is considered to be one of the promising candidate for the next generation memory device. Phase-change material, the chalcogenide alloys will be used to fabricate the memory layer of the PCM. A pulse generator is needed to induce pulses into the memory layer, for the switching process. Conventional pulse generator is quite large in size and it is difficult to control the exact value of pulse that being induced, due to the internal resistance of the connection. To overcome this problem, an integrated tuneable high speed pulse generator is needed. A tunable high speed pulse generator was designed by varying the RC circuit to have adjustable pulse width. The EDA Tools such as Mentor Graphics will be used to design the schematics and layouts. The tunable high speed pulse generator was designed by using 0.13µm technology. Pulse width from the integrated pulse generator ranging from 100µs – 100ns was induced to the PCM in order to give supply to PCM. To monitor the switching process, PCM will be connected to a simple output circuit. When the memory layer is successfully changes into crystalline phase, the LED will be 'ON' because of the current flow. When the memory is erased, which is when it changes back to the amorphous phase the LED will be 'OFF', since there will be no current flow due to the high resistance of the amorphous phase. As a conclusion, the project present an integrated circuit that helps PCM to switch phases from amorphous phase to crystalline phase or vice versa at high speed, in order to fulfill the demand of a high speed memory.**

***Keywords*— Amorphous, crystalline, Phase Change Memory, phase change material, , pulse generator.**

I. Introduction

Recently, non-volatile memory is used widely for data storage such as flash memory, FERAM and MRAM. However, these type of memory has its own disadvantages such as low speed processing to write and erase data, low scalability and less interesting for low-power consumption. Due to this problem, PCM has become the next promising technology for data storage because it has fast generation speed, high scalability, low power operation and fabrication costs. PCM can store memory because it uses the chalcogenide alloys (phase-change material) for its memory

layer. This material has two stable states which have different electrical resistance. It has the ability to switch phases from amorphous phase to crystalline phase and vice versa. When it is in the amorphous state, the resistance level is high, so it is considered as '0'. After being heated at 450 K, it will switch to crystalline with low resistance. At this state, memory is stored as '1'. The material will returned back to its normal phase, which is amorphous by being melt at 900 K and fast cooling.

Pulse generators are useful in a number of semiconductor integrated circuit devices to control time delays between operations or to control the length of an operation or a phase of that operation. The timing of operations within a memory device will be regulated by a timing pulse or other control signal generated by a pulse generator [1].

A pulse generator is needed to induce pulses into Phase Change Memory to give enough supply for it to be function. Conventional pulse generator is quite large in size and difficult to control the exact value of pulse that being induced due to the internal resistance of the connection. Therefore, on-chip pulse generator in integrated circuit would be beneficial to be design in order to give pulse widths that can be tune in order to make phase change memory to function. As for pulse generator to be tunable, for it to adjust its pulse width, the pulse generator circuit will be connected with multiple delay circuits so that tunability feature to pulse width can be obtained[1]. In order to conserve space, power and increase the operational speed of the electronic circuits, these circuits have been miniaturized by using well-known invention I.C techniques such as CMOS[2].

In the conventional practice, pulse generator is used to switch the PCM from amorphous to crystalline or from crystalline to amorphous in which the SET pulse or a RESET pulse need to be induced to the memory layer . The drawbacks of using this pulse generator are large in size and produced inaccurate pulse signal due to the internal resistance of the cable connectors. Since pulse generator are large in size, power consumption by the circuit might be large too and the operational speed of electronic circuits is slow. Therefore, tunable high speed pulse generator is needed to overcome these

This paper is about a tunable high speed pulse generator for phase change memory submitted on 31st August 2015. Accepted 20th October 2015.

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problems.

This paper is to design pulse generator circuit that can generates pulse signal with pulse width ranging from 100 µs -100 ns and design tunable high speed pulse generator with high speed, low power consumption and miniature the large size of pulse generator circuit to IC Design level. This project proposed a tunable high speed pulse generator circuit in IC Design level. The schematic of pulse generator will be drawn using Mentor Graphics Design Architect by using the Silterra 0.13 µm technology. The integrated circuit layout of pulse generator will be design using Mentor Graphics IC Station by using the Silterra 0.13 µm technology.

II. DESIGN METHODOLOGY

A. PROPOSED DESIGN FOR PULSE GENERATOR

Proposed design for pulse generator is basically using the idea of timer circuit in an astable multivibrator configuration to create stream of pulses. Fig. 1 shows the schematic of full circuit of proposed pulse generator. The timer circuit is composed of comparators, SR flip flop, and inverter.To obtain desired pulse width, the RC circuit which is externally connected from timer circuit is needed to adjust the frequency and thus adjust its pulse width. The operation of this circuit is mostly like astable multivibrator.

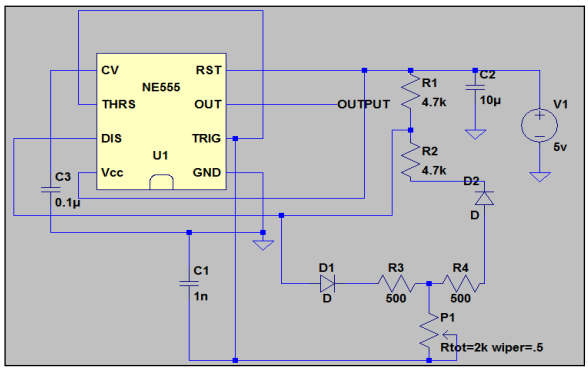

Figure 1. Full Circuit of pulse generator circuit

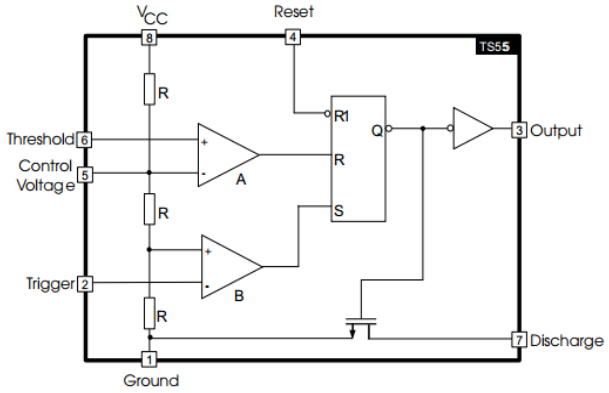

Figure 2. Timer circuit

Astable multivibrator operation does not require any external trigger to change the state of the output. External resistors and capacitor which are externally connected to the timer circuit will determined the time during which the output is either high or low. If the voltage across the capacitor is 2/3 of VDD, comparator A trigger the flip-flop and the output switches to low state. Meanwhile if the voltage across capacitor equals 1/3 of VDD, comparator B output triggers the flip-flop and the output switches to high. Then the cycle continuous. Between 1/3 and 2/3 of VDD, the capacitor is periodically charged and discharged respectively. The time during which the capacitor is charges from 1/3 to 2/3 of VDD is equal to the time where the output remains high.

Comparator B serves as input of S and comparator A serves as the input of R for the SR flip flop. From the truth table for a SR flip-flop, when input S is High(1) and input R is Low(0), the output Q of the SR flip-flop is Low(0) and the timer circuit output is High(1) due to the inverting stage.

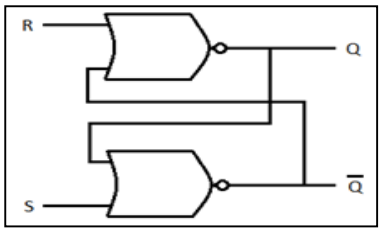

Figure 3. SR flip flop

TABLE I : SR FLIP FLOP TRUTH TABLE

SR Flip flop truth table			
Inputs		Outputs	
S	R	Q	_Q
0	0	No change	
0	1	0	1
1	0	1	0
1	1	undefined	

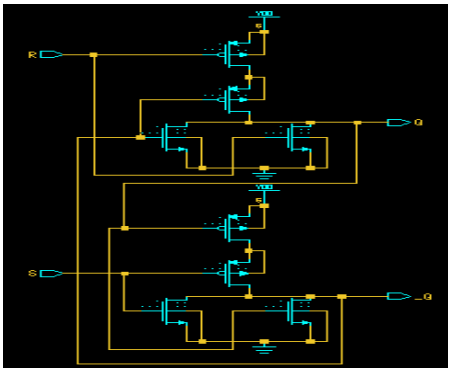

Figure 4 : SR Flip flop

Figure 4 shows that the schematic sequential circuit of SR flip flop. The sizing of SR flip flop are as follows :

TABLE II : SIZING OF SR FLIP FLOP

Transistor	W/L
M1,M2,M8,M5	4µ/0.28µ
M3,M4,M6,M7	0.52µ/0.28µ

Each of the components used in timer circuit is design and check for simulation to obtained the correct functionality of timer circuit and thus the desired pulse width can be obtained. Potentiometer is used to adjust the frequency of the circuit and thus adjust the pulse width. Based on the equation (1), the higher the frequency obtained, the smaller the pulse width.

$$f = 1 / T \qquad (1)$$

As for comparator in the timer circuit, preamplifier based comparator is used as the inputs for SR flip flop. The configuration of preamplifier based comparator are shown as in Fig. 5.

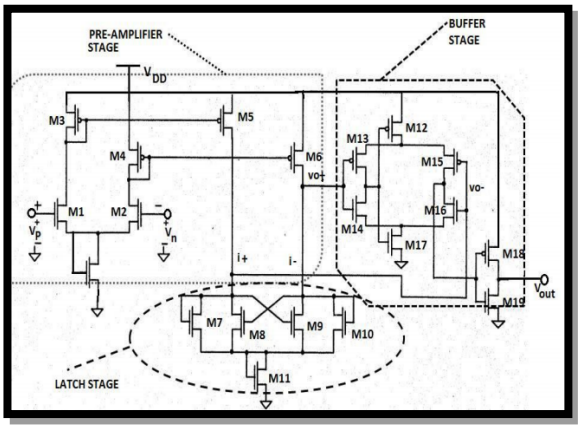

Figure 5. Preamplified based comparator

The preamplifier based comparator consist of three stages which is preamplifier, latch, and output buffer stage. Each of the transistor have been design with specific sizing. The preamplifier stage consists a differential amplifier with active loads. The preamplifier stage amplifies the input signal to improve the comparator sensitivity. It increases the minimum input signal with which the comparator can make a decision and isolates the input of the comparator from switching noise (often called kickback noise) coming from the positive feedback stage [3][4].

To determine which of the input signals is larger and amplifies its difference, the positive feedback latch stage is used. The output buffer stage consists of a self-biased differential amplifier followed by an inverter which gives the digital output. It converts the output of the latch stage to a full scale digital level output (logic 1 or logic 0).

Each of the transistor in preamplified based comparator have been design with specific sizing. Based on [9], the sizing of comparator are referred as follows :

TABLE III : SIZING OF PREAMPLIFIED COMPARATOR

Transistor	W/L
All PMOS	20µ/1µ
All NMOS	10µ/1µ

B. PHASE CHANGE MEMORY(PCM)

The concept of Phase Change Memory (PCM) using the amorphous to crystalline phase transition of cholcogenides for an electronic memory technology [5]. This material has two stable states which have different electrical resistance. It has the ability to switch phases from an amorphous phase to crystalline phase and vice versa.

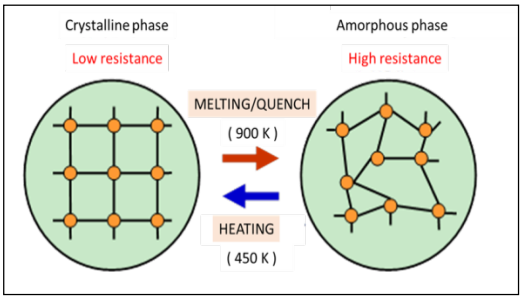

Figure 6.Structure molecule of PCM

The amorphous phase the value of resistance is high and at the crystalline phase the value resistance is low. The phase change memory (PCM) exploits the large resistance contrast between the amorphous and crystalline state in a so-called phase change material. The amorphous phase tend to have high electrical resistivity, while the crystalline phase exhibits a low resistivity, sometimes 3 or 4 orders of magnitude lower [6]. These two states are characterized by remarkably different resistance levels; an amorphous material has high resistance, usually in the MΩ range, where crystalline material has low resistance, usually in the kΩ range [7].

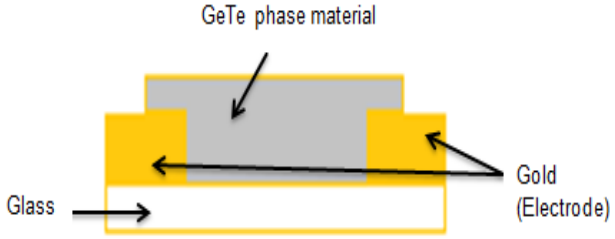

Figure 7.Structure of Sample

The material that used for this project is Germanium Tellurium (GeTe) phase material. This switching process is

achieved by simulating the cell with suitable electrical pulses that appropriately heat the material, triggering the phase-change. In the conventional practice, the pulse generator is used. The pulse generator will produce a square wave as the electrical signal input to the PCM to change from an amorphous phase to crystalline phase.

C. OVERALL SYSTEM

The scope of this project are to design a tunable high speed pulse generator circuit using Mentor Graphics to design it. Phase Change Memory will be fabricated with **chalcogenide alloys** for an optimize structure for data storage and the integration between pulse generator circuit and the fabricated PCM.

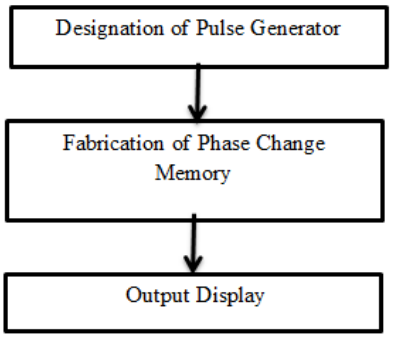

Figure 8. Block Diagram of the System

Fig. 8 shows that the block diagram of the system. At first the designation of pulse generator. The high speed pulse generator will generate suitable electrical pulses that appropriately heat the material of the memory layer, triggering the phase-change power supply to the phase change memory (PCM). The electrical pulses from pulse generator can be control by tuning the potentiometer to adjust the pulse width with value ranging from 100µs to 100ns. When the memory layer changes into crystalline phase, the LED at the output circuit will be 'ON' because of the current flow due to low resistance. When it switches back to the amorphous phase, resistance will be high, resulting to no current flow and the 'LED' will be 'OFF'.

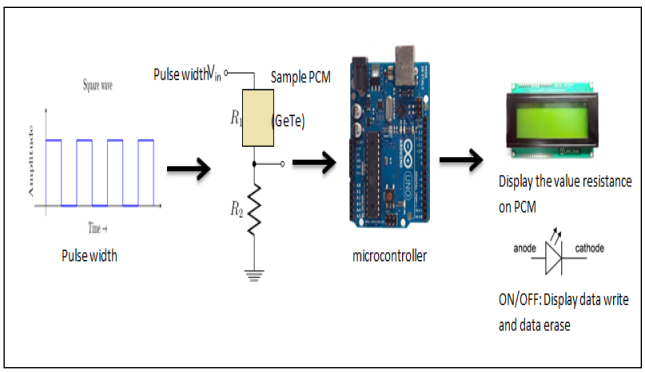

Figure 9. System to display value resistance for PCM

Fig. 9 shows that the circuit to display the value of resistance for PCM. The input for this circuit is pulse width that generates from pulse generator circuit. This circuit is connected to the microcontroller. The principle of this circuit uses voltage divider circuit as in (2), that one of the resistors will replace with sample PCM (GeTe).

$$V_{\text{out}} = \frac{R_2}{R_1 + R_2} \cdot V_{\text{in}} \qquad (2)$$

To solve for R1, referring to (3):

$$R_1 = \frac{R_2 \cdot V_{\text{in}}}{V_{\text{out}}} - R_2 = R_2 \cdot \left(\frac{V_{\text{in}}}{V_{\text{out}}} - 1\right) \qquad (3)$$

At the amorphous material, the value of resistance for PCM is high, usually in the MΩ range. The LCD will display value resistance in MΩ range and LED will 'OFF' that means data erasing. When supply the pulse width, the amorphous material will change to crystalline material and this material has low resistance, usually in the kΩ range. At this stage the LCD will display resistance in kΩ range and the LED turns 'ON' that means write data.

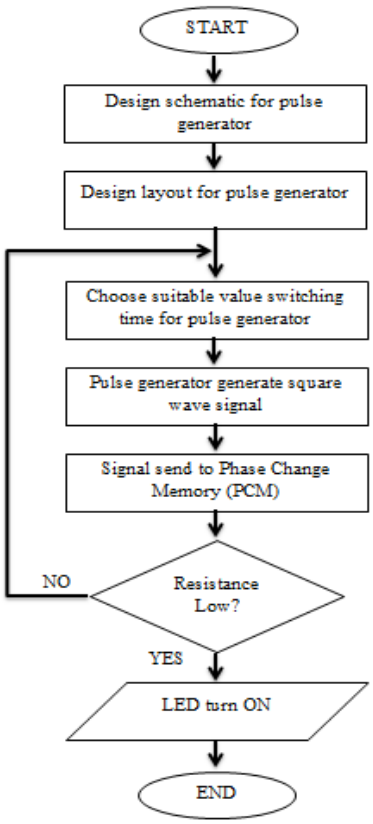

Figure 10. Flowchart for operation of the system

III.RESULT AND DISCUSSION

A. PULSE GENERATOR

Before proceeds to the designation in mentor graphics, the circuit of pulse generator is simulate using LTSpice to check whether the pulse generator circuit is able to generate pulse width ranging from 100µs-100ns or not by varies the resistances and capacitors value. Once the pulse generator is able to generate pulse width the resistor and capacitor is identified on which can produce desired pulse width. Fig 11. shows that the simulation for pulse width that been generated by pulse generator.

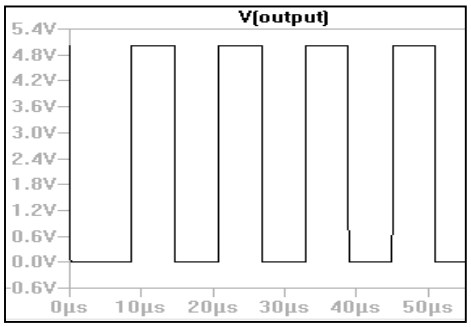

Figure 11. Simulation for pulse generator circuit using LTSpice

TABLE IV. SIMULATION (LT SPICE) AND EXPERIMENTAL RESULT FOR CAPACITOR 1NF

R1 (Ω)	C1 (F)	Simulation	Experiment
2k	1 n	5.87 µs	6.60µs
4k	1 n	7.07 µs	8.40 µs
6k	1 n	7.89 µs	9.20 µs
8k	1 n	8.69 µs	10.20 µs
10k	1 n	9.82 µs	12.20 µs
20k	1 n	9.72 µs	18.40 µs
30k	1 n	19.04 µs	25.60 µs
40k	1 n	23.42 µs	43.60µs

TABLE V. SIMULATION (LT SPICE) AND EXPERIMENTAL RESULT FOR CAPACITOR 10NF

R1 (Ω)	C1(F)	Simulation	Experiment
2k	10 n	59.14 µs	50.00 µs
4k	10 n	68.48 µs	62.00 µs
6k	10 n	77.86 µs	74.00 µs
8k	10 n	87.47 µs	86.00 µs
10k	10n	96.56 µs	140.00 µs
20k	10n	143.40 µs	160.00 µs
30k	10n	188.00 µs	200.00 µs
40k	10n	143.20 µs	400.00 µs

Table IV and V shows that the comparison between simulation using LTSpice and experiment for pulse generator when R1 is varies and the value for C1 = 1nF and 10nF. The pulse width value obtained shows that the circuit can produce pulse width ranging from 100µs-100ns.

Proceed to the designation of pulse generator circuit in Mentor Graphics using 0.13µm technology. Each component in the timer circuit is simulate and check whether it is working as follows in the theory or not. For comparator, the transient analysis is obtained to see the functionality of the comparator. Transient analysis of comparator is shown at Fig. 12.

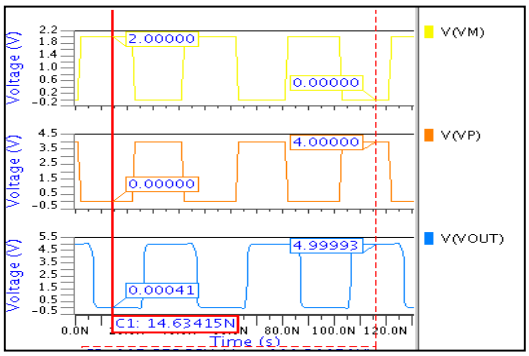

Figure 12. Transient Analysis for comparator

Based on the result obtained for transient analysis of preamplified comparator, when Vp is greater than Vm, the output will be HIGH which means it follow VDD. Meanwhile when Vm is greater than Vp, the output will be LOW. The simulation obtained are the same as theoretically, thus the comparator is functioning well. This is because that when Vp is set smaller than Vm, the output become LOW as what in the theoretical and vice versa.

Once the component in timer circuit is correctly function, the timer circuit will be design as in Fig. 13.

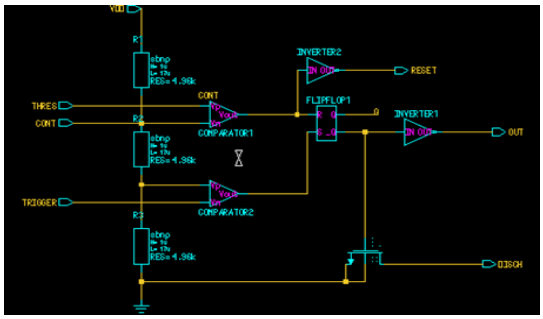

Figure 13. Schematic of timer circuit

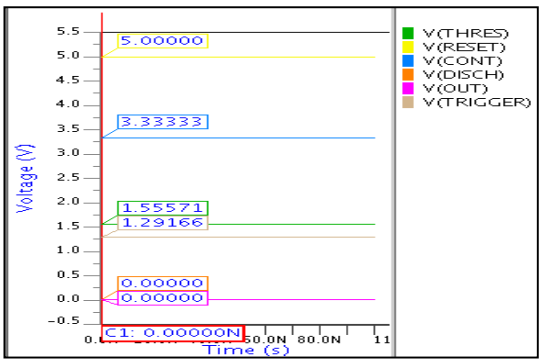

Figure 14. Output of each voltage of timer circuit

Fig. 14 shows that the output of timer circuit which almost the same as the real timer circuit NE555. The specification of parameters are obtained as in Table VII.

TABLE VI. COMPARISON OF SIMULATION IN LTSPICE AND MENTOR GRAPHIC

Voltage	Mentor Graphic	LTspice	Datasheet NE555
Vcont	3.33V	3.33V	3.3V
Vthres	1.56V	0V	3.3V
Vtrigger	1.29V	0V	1.67V
Vdischarge	0V	0V	0.15V
Vreset	5V	4.8V	0.7V

Table VI shows that the parameter of timer circuit that been obtained when simulate in mentor graphic and LTspice software to compare the functionality timer circuit of NE555 that been design whether it is the same or not. The values of Vthreshold and Vtrigger might not getting the same as in LTspice simulation due to error in the circuit.

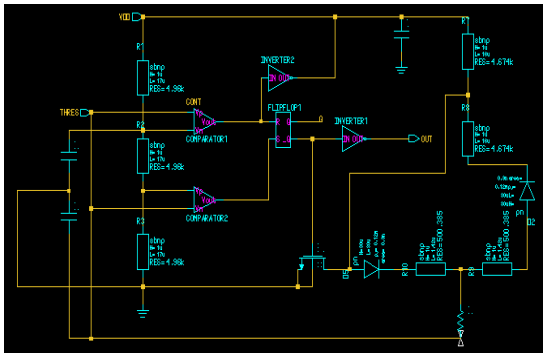

Figure 15. Schematic for full circuit pulse generator with tunable part

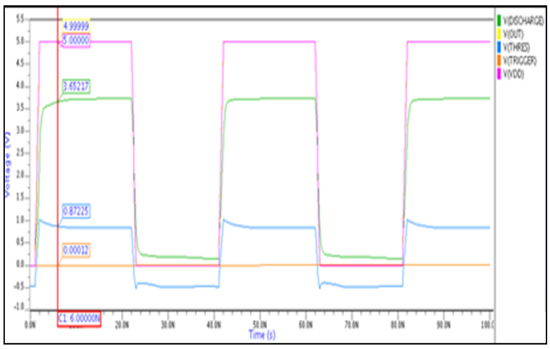

Figure 16. Transient analysis for full circuit pulse generator

Fig. 16 shows that the transient analysis for full circuit of pulse generator. The circuit is able to generate pulse width waveform however due to some error when varies the resistor and capacitor, the value of pulse width is not changing. The pulse width remain the same when changing the resistor and capacitor value in simulation.

B. PHASE CHANGE MATERIAL

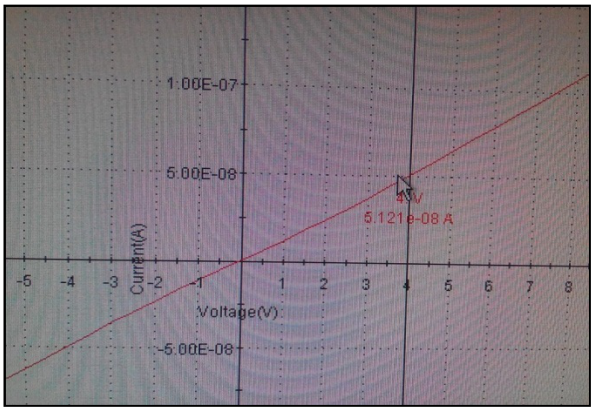

Figure 17. The I-V measurement without pulse

Fig. 17 shows that the result of the I-V measurement of the PCM sample. The value of the resistance above is in MΩ. MΩ is representative for the amorphous state. When the pulse is supplied from the pulse generator, the value of the resistance must be changed to the kΩ. kΩ is representative of crystalline state. The value of the resistance without pulse is 78.11 MΩ.

TABLE VII. RESULT WITHIN PULSE

Voltage (v)	Pulse Width (μs)	Resistance (ohm)
0.5 to 5	100	Does not change
0.5 to 5	200	Does not change
0.5 to 5	300	Does not change
0.5 to 5	400	Does not change
0.5 to 5	500	Does not change

Table VII shows that the result of the resistance after the pulse is supplied from the pulse generator. The range of the voltage that used in this experiment from 0 to 5V are same for all the pulse width. There are no changes of the output resistance when the pulse is supplied. The output resistance is same within and without the pulse. These kind of the problem occurs due to the size of the sample, thickness of the thin film and the distance between the electrode and the GeTe material. The major problem that occurs in this experiment is the PVD machine to deposit a new sample does not function well. It is still in the progress to create a new sample until the PVD machine is in the right condition.

C. MEASUREMENT OF OVERALL SYSTEM

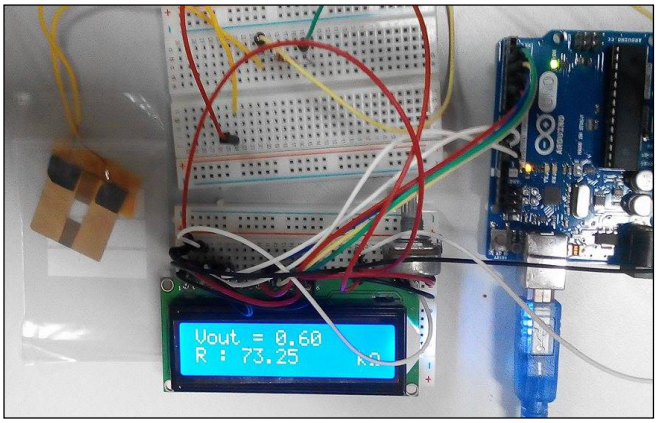

Figure 18. Display the value of resistance

Fig. 18 shows that the value resistance of sample phase change material on the LCD. The sample at crystalline stages because the value resistance show in kΩ value. When the sample at amorphous stages, the value of resistance will display in MΩ range.

IV. CONCLUSION

As conclusion for this project, the PCM is able to change its phase from amorphous to crystalline and vice versa through heating process. The changes of the phase is measured through the IV- measurement. The amorphous state represent the value of the resistance in mega ohm and the crystalline state represent the kilo ohm. The changes of the state is shown by the changes in the graph. As for the pulse generator circuit, it was simulated in mentor graphic using 0.13µm technology. The timer circuit of main circuit in pulse generator circuit is able to generate almost the exact value like the NE555 timer circuit. The tunable pulse generator circuit is able to generate certain pulse width ranging from 100µs to 100ns. The simulation in LTSpice is done in order to get the pulse width varies by resistor and capacitor also the model of circuit hardware of proposed pulse generator is done to get the pulse width. For the whole system integrating PCM and pulse generator, when pulse supplied by the pulse generator however is not enough due to the size of sample for phase change memory fabricated is large, the changing state for PCM is not occur. The size of sample should be in smaller size in order for it to receive enough pulse signal from the pulse generator.

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