Characterization and Fabrication of 90nm Strained Silicon PMOS using TCAD

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***Abstract*—The paper focuses on the enhancement of conventional 90nm PMOS using graded silicon germanium layer (SiGe) within the channel and bulk of semiconductor. The performance of conventional 90nm PMOS and 90nm PMOS with silicon germanium layer was compared. A process simulation of Strained Silicon PMOS and its electrical characterization was done using Silvaco TCAD tool. The analysis focused on Id-Vg and Id-Vd characteristic, and hole mobility changes. With the Germanium concentration of 35%, the threshold voltage Vt for the strained Si and conventional PMOS is -0.228035V and - 0.437378V respectively. This indicates that the strained silicon had lower power consumption. In addition, the output characteristics obtained for Strain Silicon PMOS showed an improvement of the drain current as compared with conventional PMOS.**

***Index Terms*— Strain silicon, SiGe, PMOS devices, Simulation**

I. Introduction

INCREASING microprocessors performance and rapid growth of the information technology revolution was due to rapid scaling of MOSFETs. The underlying principle behind the revolution is Moore's law. In 1965, Gordon Moore observed that the number of transistors in a chip increased exponentially and the transistor size decreases exponentially over time. When Moore made his prediction in 1965, transistor size was 100 m. During the last three decades, Moore's prediction has held as transistor size exponentially decreased from micrometers to submicrometers and then to deep submicrometers [1]. Presently, with the introduction of 90-nm CMOS logic technologies and 45-nm transistors in 2003, Moore's law is found to still be valid in the nanotechnology era.. Moore pointed out that reduced cost per function is the driving force behind the exponential increase in transistor density. It is this exponential reduction in cost per function that drives microprocessor performance and growth of the information technology and semiconductor industry. Strained silicon is one of those rare new technologies that enables a fairly dramatic increase in performance with a relatively simple change in starting materials. Proof that transistors fabricate PMOS with strained silicon were faster due to increased electron mobility and velocity was first demonstrated in the mid-1980s. Then, in 1998, researchers showed it would work with leading-edge, sub-100 nm short-channel transistors. Today, companies such as Intel, IBM, Hitachi, AMD and UMC have reported success with strained silicon.

Strained silicon works by growing a thin layer of silicon on top of a layer of silicon germanium. There are two major types of induced strain that can be introduced in CMOS technologies for carrier mobility enhancement which are biaxial and uniaxial strain. Longitudinal tensile strain (strain along the channel, making it longer) allows holes to move more quickly and smoothly. In biaxial tensile strain, the interatomic distances in the silicon crystal are stretched, generally increasing the mobility of holes making p-type transistors faster [2].

The strained – Silicon is produced by depositing a thin layer of Silicon on silicon germanium layer onto a Si substrate . The top Si layer is strained at the Si and SiGe interface because lattice of SiGe exerts a strain on the thinner top Si layer, stretching the Si layer slightly. Further, by controlling the amount of Ge in the bottom SiGe layer , the amount of strain produce in the overlying Si Layer can be manipulated. The atoms in the silicon layer align with those in the slightly larger crystalline lattice of the SiGe (germanium atoms are larger than silicon). Fig. 1 shows silicon germanium (SiGe) is placing under the silicon crystal. When the SiGe deposited to the silicon crystal, the structure of silicon crystal will strain due to wider distance of SiGe lattice.

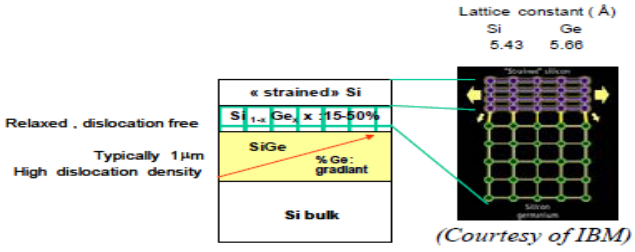

Fig. 1. Straining silicon requires several epitaxial steps: a SiGe buffer on bulk Si; a relaxed SiGe template on the buffer SiGe; and Si on the relaxed SiGe template, which strains this top layer of silicon.

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It was discovered that the lattice mismatch between Si and Ge atoms could be accommodated by a finite degree of lattice distortion. This distortion or strain actually offers the advantage of allowing electrons and holes to move faster. This increase in carrier mobility is attributed to a modified Si Band structure that lowers the resistance to electron and holes to movement in the material. The result is increased hole mobility in PMOS and electron mobility in NMOS devices. This leads to an increase in channel drive current and also some reductions in power consumption. [3-6].

This research is to study the effect of silicon germanium layer in the channel and to show the enhancement in drive current due to incorporation of SiGe/Si heterostructure channel. Besides, this research also to investigate the effect of strained Si on hole mobility.

II. Device Doping Profile

Fig. 2 shows the net doping and Ge concentration profile for the SSPMOS. This is the result from the Athena simulation by performing a vertical cutline which starts at the gate and stops at the substrate. From Fig. 2, we can see that the boron doping is high at the gate with 1 x 10^{20} cm^{-3} doping concentration. There is no doping in the silicon dioxide layer. Meanwhile the phosphorus doping at the strained silicon, SiGe layer and substrate is 1 x 10^{16} cm^{-3}. The composition x shows a 0.35 of Ge concentration in silicon germanium layer only.

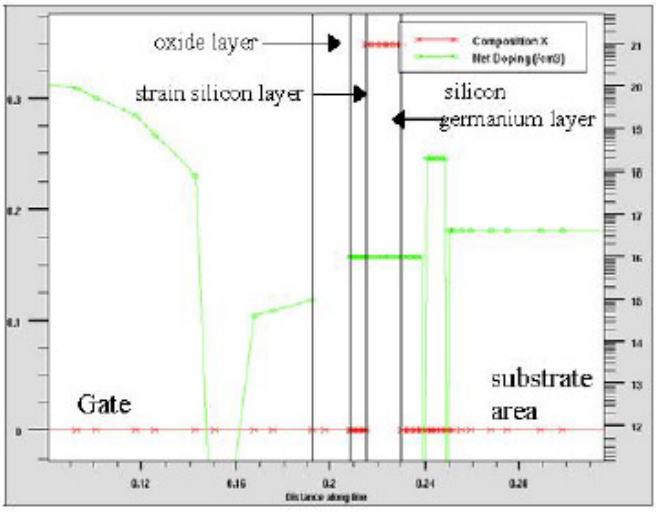

Fig. 2: The net doping and Ge concentration profile for SSPMOS.

III. Procedure

A. Device Structure and Process

Both strained silicon PMOS with an added SiGe layer and normal conventional PMOS device without SiGe layers process simulation were carried out using ATHENA, The simulation process to create the strain silicon PMOS is similar to the conventional PMOS fabrication process. The fabrication of conventional 90nm PMOS device starts by creating an initial silicon substrate p-type with phosphorus doping of 2 x 10^{18} cm^{-3}. Next, we perform diffuse process to grow oxide with thickness 0.367717 um. The process continues with the implantation of Boron 1 x 10^{18} cm^{-3} for adjust threshold voltage. Polysilicon is then deposited and patterned to form the gate. Next the silicon nitride (Si3N4) layer is deposited and patterned for spacer formation. Then the aluminum is deposited and patterned to act as the metal contact

Finally, the final structure of the conventional 90nm PMOS is shown in Fig. 3. The difference between the conventional structure with the Strain Silicon PMOS structure is that there is no added SiGe layer. The Strain Silicon PMOS structure is created with the thickness 0.010 µm is deposited on the silicon substrate. Then a silicon germanium (SiGe) layer with the thickness of 0.015 µm is deposited on the silicon layer, followed by deposition of another silicon layer with 0.007 µm thickness to the SiGe layer. After the deposition, strained silicon is created at the channel. In Strained Silicon PMOS, the fraction concentration for gemanium content in SiGe chosen to be 0.35 meanings that 35% of SiGe consist of germanium material and the dopant impurity of boron to 3e15 atom/cm3. This syntax was included in Athena input file:

"deposit silicon thick=0.010 divis=4 c.phos=1e16"
"deposit sige thick=0.015 divis=5 c.frac=0.35 c.phos=1e16"
"deposit silicon thick=0.007 divis=4 c.phos=1e16"

ATLAS was used as device simulator to measure electrical characteristic of each device. In order to find Id-Vg characteristics, Vg was varying from 0V to -1.2V with constant value of Vd that is 100mV.

For Id-Vd characteristics, both structures are simulated to ramp the drain voltage, Vds to 100mV when the gate voltage, Vgs is bias to -0.5V, -0.8V and -1.1V V. These two devices tested with the same condition to observe electrical characteristic and differentiate between PMOS SiGe and without SiGe. Then the carrier mobility between conventional PMOS and PMOS using SiGe was compared by using equation (1) below :

$$Id_{sat} = \frac{\mu C_{ox}}{2L}\left(v_{gs} - v_t\right)^2 \quad (1)$$

- Process fabrication flow:
  - According to device specification

TABLE I
CONVENTIONAL 90nm PMOS

No	Process	Material/Dose/Dimension
1	Initial substrate	Phosphorus 2e18 atoms/cm^3
2	Threshold Voltage Adjust	Boron 1e18 atoms/cm^3
3	Gate oxide	Deposit Gate Oxide
4	Polysilicon gate	90nm length
5	Spacer formation	Deposit nitride
6	Source drain implantation	Boron 1e15 atoms/cm^3 20kev
7	Metallization	Deposit Aluminum

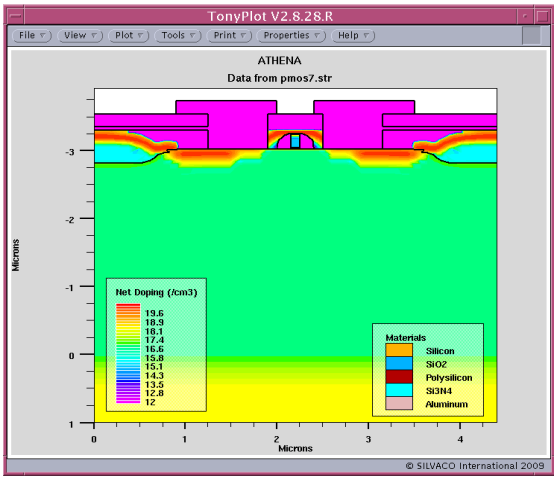

Fig. 3 Cross section of Conventional 90nm PMOS

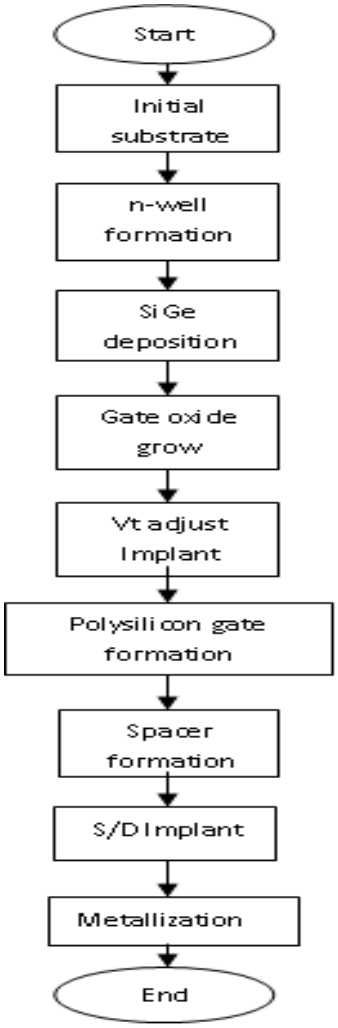

Fig. 4: Process Flow for SiGe PMOS

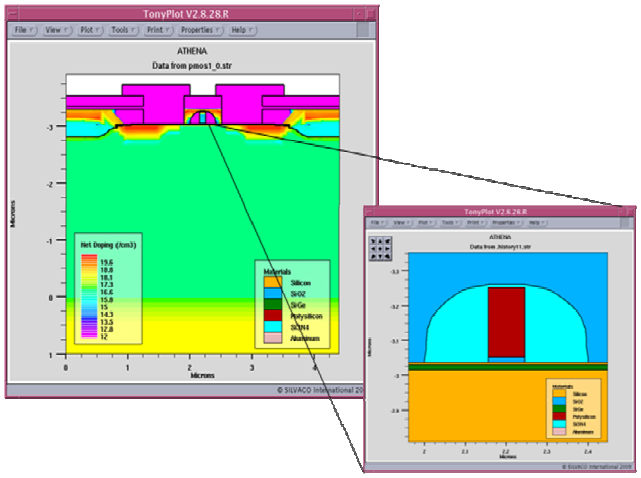

Fig. 5 Cross section of 90nm SiGe PMOS

B. Electrical Characterization

In device simulation, both the strained silicon structure and the conventional PMOS structure are simulated in Atlas. The devices are simulated to obtain the characteristics of the conventional PMOS and strained silicon PMOS (SSPMOS). The mobility models that are used to obtain the electrical characteristics are the parallel electric field dependence and concentration dependent model. Beside that, the carrier static lifetime for the Si material is set at le-7 tau for electron and hole. Meanwhile the SiGe material is set to le-8 tau for electron and hole. For the carrier statistic model, the bandgap narrowing and Boltzman are chosen in this simulation. As for the recombination models, the auger and SRH concentration dependent lifetimes are chosen. The characteristics of the devices that was obtained from the simulation are the drain current versus gate voltage curve, threshold voltage, drain induced barrier lowering (DIBL) and drain current versus drain voltage curve.

C. Mobility Enhancement With Strained-Si

A key scaling problem in nanoscale transistors is the mobility degradation caused by the large vertical electric fields. Fig. 6 shows the mobility versus technology scaling trend for various Intel process technologies. It is shown that the mobility has decreased from 400 to 120 cm Vs during the last decade. It is becoming increasingly important to incorporate mobility enhancing process features in nanometer logic technology to counteract this undesirable mobility trend [7-8].

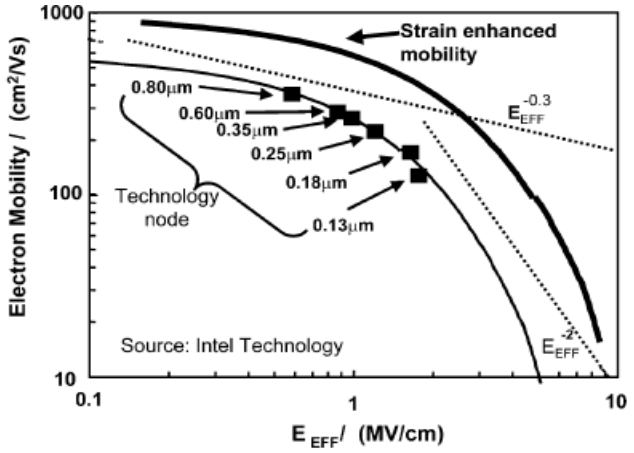

Fig. 6.Mobility versus technology scaling trend for Intel process technologies.

1) Strained-Si Hole Mobility Enhancement:

The mobility for the short channel device is extracted from the improvement in the linear current [1] using:

$$I_D = I_0(V_{CS} - V_T)(V_{DS} - I_D R_{SD})(V_{DS} = 50mV) \qquad (2)$$

Where R_{SD} is measured independently. The field dependence of the mobility is also extracted using conventional techniques on a long channel transistor [1] where is negligible to validate the field dependence is correct Summarizing references [10]–[16], the strain enhanced hole mobility understanding has lagged behind electron [14], [17] and much of the understanding, has first been driven by experimental data. There have been few theoretical hole mobility studies due to the complicated nature of the valence bands not amenable to a simple analytic description [17].

Fig. 7 summarizes what is known about the hole band structure for unstrained and strained-Si. The valence bands are plotted for the in-plane direction of the MOSFET. Both uniaxial and biaxial stress lifts the degeneracy n the valence band and causes shift and warping of the bands as shown in Fig. 7. For both types of stresses, holes populate the lowest energy band which is light-hole like. Considering the mobility enhancement at low strain results from in-plane conductivity effective mass changes, the biaxial tensile and longitudinal uniaxial compressive stress mobility data suggest the uniaxial stress band warping and repopulation creates a significantly lower in-plane mass. Evidence of a low in-plane effective mass (high mobility) for uniaxial stress exists in the literature and was first calculated by Bir and Pikus in 1958 in which a "dimple" at k = 0 is formed by the light-hole band dropping in energy [10], [11].

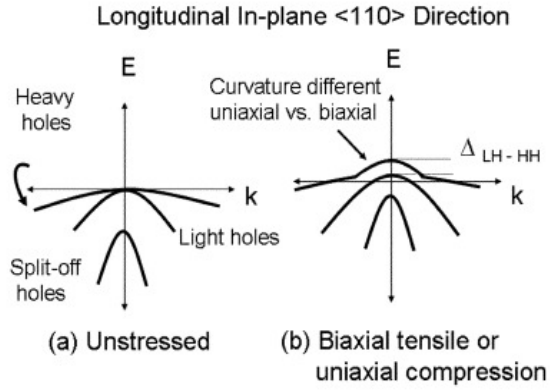

Fig. 7. Hole mobility for uniaxial strained-Si introduced Si Ge in the source and drain [9].

Next, we summarize what is known about the field dependence of the hole mobility. For biaxial stress, Fischetti showed the loss in enhanced hole mobility results from reduced separation between the light and heavy-hole like bands (see Fig. 7) with increased vertical field [14]. Based on the experimental hole mobility enhancement in this work, the confining surface potential does not reduce the strain induced band separation for uniaxial compressive stress. The reason the separation is not lost for uniaxial stress must again be caused by bandwarping creating an advantageous (large) out-of-plane effective mass for the top energy band [18-20].

IV. RESULTS AND DISCUSSION

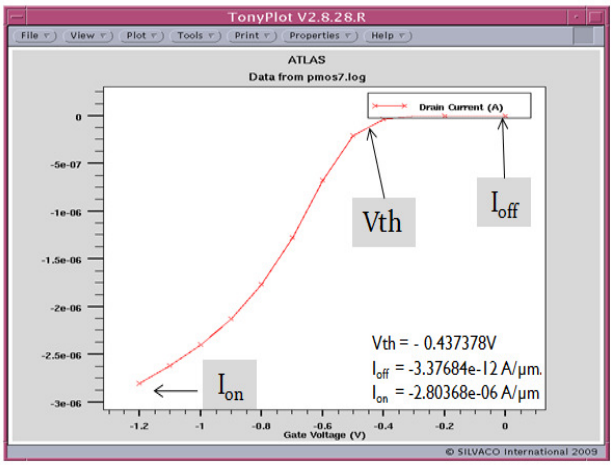

Fig. 8 : Id-Vg curve for Conventional 90nm PMOS

From the simulation, the drain current, Id versus gate voltage, Vgs curve with a drain voltage, Vds of 100mV for conventional PMOS. The measured threshold voltage was -0.437378V with optimized Vt adjust of 1.0e18 atoms/cm3 Boron material as illustrated in Fig. 3. Ion was measured to be 2.80368e-06A/um while Ioff -3.37684e-12 A/um.

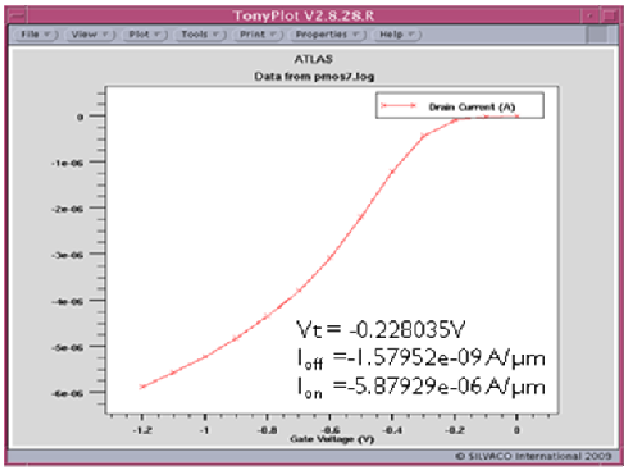

Fig. 9 : Id-Vg curve for 90nm PMOS SiGe

From the Fig. 9, Vth for PMOS using SiGe was reported to be -0.228035V with Ion and Ioff equal to -5.87929e-06 A/um and -1.57952e-09 A/um respectively. The measurement shows that PMOS SiGe provide higher Idmax (Ion) compared to conventional PMOS and higher current leakage (Ioff) during the same test. From the result show that the drain current for Strain Silicon PMOS structure is higher than conventional PMOS. This indicates that the Strain Silicon PMOS has higher drive current compared to conventional PMOS. Meanwhile the extracted threshold voltage are -0.228035V and -0.437378V for the Strain Silicon PMOS and conventional PMOS respectively. This indicates that the strained PMOS has lower voltage threshold than the conventional PMOS which translates to lower power consumption.

This result shows that the silicon beneath the gate experience compressive stress during ion implantation process forming source and drain. Essentially SiGe layer will relax the thin silicon as shown in Fig. 5 which compressive stress was expected to induce by dopant concentration during ion implantation process. Since the thick silicon under the gate experience compressive stress cause the inter-atomic distances are shortened and it allow heavy hole to move easily through the structure . This will increase the mobility of hole and drain current and thus improving transistor switching speed. Differently with NMOS that consist of electron as majority carrier that can increase the drain current when experience tensile strain because the inter-atomic distances of this structure are larger and allow light electron to move faster and improve the performance of NMOS.

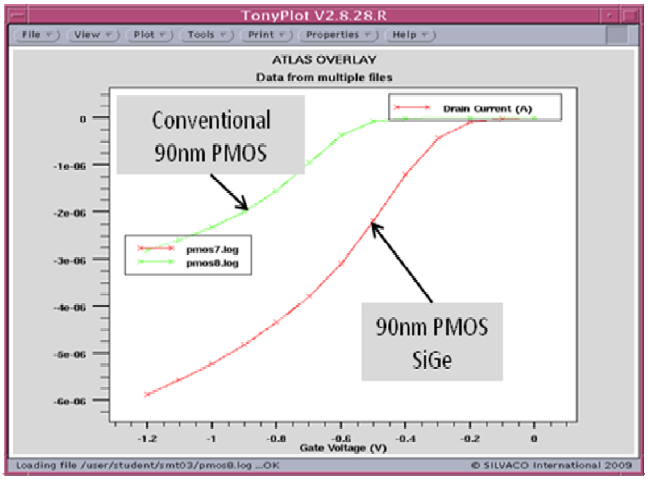

Fig. 10. ATLAS overlay (Id-Vg)

- The silicon under the gate experience compressive stress during ion implantation process source and drain.
- Essentially SiGe layer will relax the thin silicon which compressive stress was expected to induce by dopant concentration during ion implantation process.
- Since the thick silicon under the gate experience compressive stress cause the inter-atomic distances are shortened and it allow heavy hole to move easily through the structure
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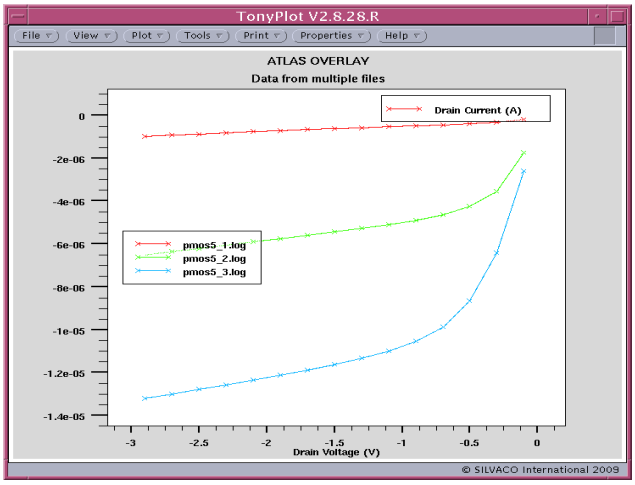

Fig. 11: Id-Vd curve for Conventional 90nm PMOS

Beside that, conventional PMOS structures was simulated to ramp the drain voltage, Vds to 100mV when the gate voltage, Vgs is bias to -0.5V, -0.8V and -1.1 V. The simulation results are presented in Fig. 11 which represents the graph of the drain current versus the drain voltage. From The simulation, with the test voltage at Vg=-1.1V resulted Idmax to be -1.32052e-05 A/um

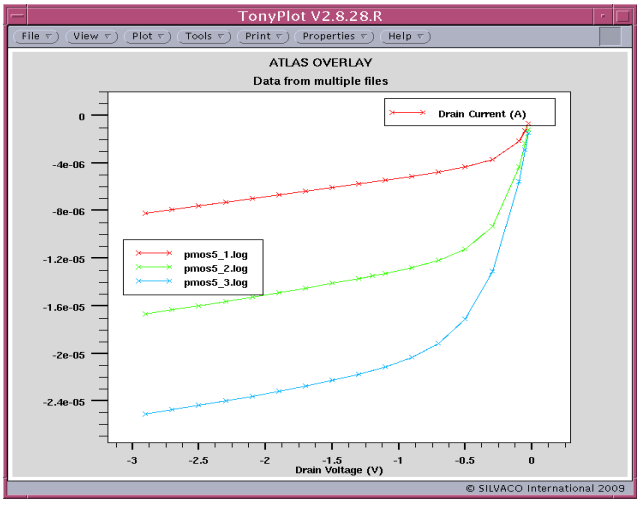

Fig. 12: Id-Vd curve for 90nm PMOS SiGe

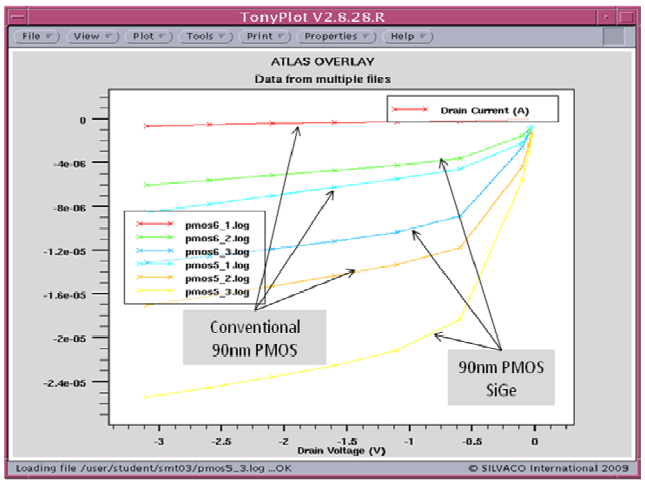

Fig. 13. ATLAS overlay (Id-Vd)

Since Id-Vg curve show the increase of Idmax, same goes to the Id-Vd for the same gate voltage using SiGe as illustrated in Fig. 12. This proves that with the test voltage at Vg=-1.1V resulted Idmax to be -2.50815e-05 A/um. From Fig. 6, it can be seen that the strained PMOS device has a higher drive current as compared to the conventional PMOS. From these results, it is evident that the strained silicon PMOS has a better performances than conventional PMOS.

MOS devices that feature strained-Si regions in the channel area are attracting significant interest as dramatic improvement of the electrical characteristics relative to conventional devices that has been reported in strained channel MOS transistors.

V. CONCLUSION

it can be seen that the Strain Silicon PMOS has better performance compared to conventional PMOS. This can be shown from the comparison result between both structure in electrical characteristic of each Id-Vg and Id-Vd. The results also has shown that the significant increase of hole mobility and drain current as compared to conventional PMOS. It shows that 90nm PMOS using graded silicon germanium on the channel is suitable to improve the performance of PMOS.

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