Delta Sigma Digital Analog Converter Circuit Design for Neurochemical Sensing

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Abstract— **The aim of this project is to measure dopamine signal current via In Vivo Voltammetry System. Voltammetry is a category of electroanalytical methods used in analytical chemistry. In voltammetry, information about an analyte is obtained by measuring the current as the potential is varied. In Vivo Voltammetry is used to measure dopamine signal current when potential applied to the dopamine while subject still alive. In Vivo Voltammetry system consists of several parts such as Op-Amp, Voltage Frequency Converter, Digital Analog Converter and Potentiostat. Specifically, this project is to design and simulate a Digital Analog Converter (DAC) by implementing Delta Sigma Modulator. Simulations are done in PSpice software. Delta Sigma DAC is chosen to meet the desired voltage output 900mV and frequency 4Hz. This type of DAC is different from other common used DAC because it provides high resolution for accuracy implementation. Potentiostat requires voltage supply from a high resolution, accurate and low speed DAC.**

Index Terms— **Digital Analog Converter, Delta Sigma Modulator, In Vivo Voltammetry System**

I. Introduction

NEUROCHEMICAL sensing is a rapid sensing technique that can directly detect neurotransmitters change in neurochemical monitoring. A neurochemical is an organic molecule, such as dopamine or nerve growth factor that participates in neural activity. Neurotransmitters are chemicals which relay, amplify and modulate signals between a neuron and another cell. Examples of neurotransmitters are dopamine, glucose, glutamate, etc. These neurotransmitters can be found in brain. Dopamine plays important roles in behavior and cognition, motor activity, motivation, sleep and mood. Low concentration of dopamine in human brain could lead to Parkinson disease [5].

Recent projects have developed in vitro voltammetry as a technique for rapid measurement of dopamine in the brain of freely behaving rats. However, in vitro system measurement has several limitations. It is a bulky measurement system and has restriction of cables connecting the head assembly of rat to the measuring systems. Therefore, in vivo system measurement is a solution to the in vitro system limitations [1].

In Vivo Voltammetry is a powerful method of recording changes in extracellular transmitter concentration in unrestrained animal and may be applicable to human. This voltammetry system has several significant contributions in medical area. It can improve current system of hospital care. For example, patients can stay at home as soon as they can walk or be wheeled out the door because their health condition can be monitor by hospital virtually. Thus, reduce the cost of health care. Furthermore, it cans improved life by letting patient and clinician know when and how to adjust drugs dosage to optimize treatment.

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A. *In Vivo Voltammetry System*

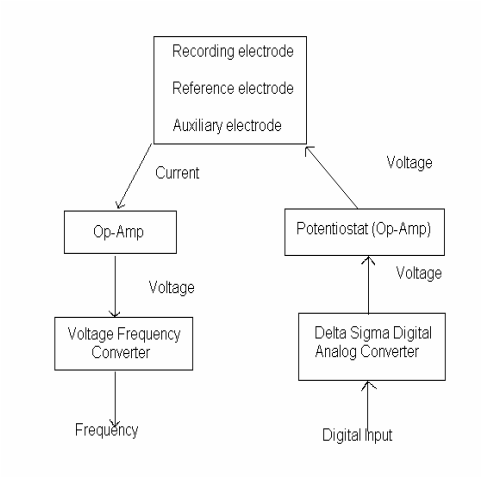

Fig. 1. General Block Diagram of In Vivo Voltammetry System

The general block diagram of In Vivo Voltammetry System was shown in Figure 1. The voltammetry system operation initially begins at three types of electrodes. Recording electrode is in contact with dopamine and applies desired voltage. Reference electrode act as reference in measuring and control recording electrode. Auxiliary electrode pass current needed to balance the current observed at recording electrode. Dopamine produces chemical reaction while applying small voltage potential value. Current in nanoAmpere (nA) is measured every 0.25s. The measured current is proportional with dopamine concentration.

Then op-amp will convert the current to be a voltage. Next, Voltage Frequency Converter converts voltage to pulse frequency. Digital Analog Converter (DAC) converts digital input to voltage. Potentiostat control the small voltage applied to electrode. It keeps the potential of the working electrode at a constant level with respect to the reference electrode [1].

B. *Delta Sigma Digital Analog Converter*

Digital-to-analog converter (DAC) is a device for converting a digital (binary) code to an analog signal (current, voltage or electric charge).There are several types of DAC such as Binary Weighted DAC, R-2R Ladder DAC and Delta Sigma DAC[3]. Delta Sigma DAC can be designed to suit high voltage resolution requirement in low frequency compared to other DAC.

The Binary Weighted DAC has limitation which is there is large difference in resistor values between Most Significant Bit (MSB) and Least Significant Bit (LSB). For example if the MSB resistor is 1kΩ in 10 bit DAC, the LSB resistor is 1.024MΩ. With the current IC fabrication technology, it is very difficult to produce resistance values over a wide resistance range.

There is also limitation to used R-2R Ladder DAC. It uses a repeating cascaded structure of resistor values R and 2R. This improves the precision due to the relative ease of producing equal valued matched resistors. However, wide converters perform slowly due to increasingly large RC-constants for each added R-2R link.

Delta sigma DAC converts digital input (binary) to analog output (voltage). Delta-sigma circuit has two main sections which are delta section and sigma section. Delta receives incoming digital signal and monitor outgoing pulse train. It creates error signal which is the difference between binary signal coming in and pulse train going out. Sigma adds up the result of error signal created by delta and supplies sum to the low pass filter.

The objectives of this project are to design and simulate Delta Sigma Digital Analog Converter using Orcad PSpice and to meet the desired Delta Sigma DAC voltage output 900mV and frequency 4Hz with a resolution of 50mV.

II. METHODOLOGY

Circuit is designed based on Delta Sigma Digital Analog Converter by implementing Delta Sigma Modulator. The circuit is designed according to Delta Sigma DAC block diagram and project's requirements. The circuit is prepared in Schematic Capture of Orcad P-Spice.

Then, the sub circuit is simulated to determine whether each sub circuit produce the desired output. The complete circuit is simulated only when all sub circuit functions well. Simulation is essential to verify that the design circuit is applicable and can be operated. It is also useful to know whether desired output is established.

Finally, the result is display after circuit simulation successfully completed. The output result and circuit operation flow can be visualized in graphs, charts and figures [4]. The output results from PSpice simulation are analyzed. Methodology stage is shown in Figure 3.

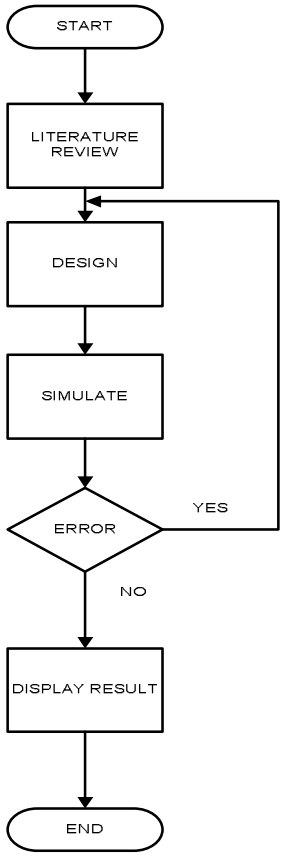

Fig. 3. Progress Flow Chart

The Delta Sigma DAC block diagram as shown in Figure 4 can be divided into several parts which are register, subtractor, adder, one bit DAC and low pass filter. The operation of Delta Sigma DAC block diagram begins with digital samples (A) is fed into subtractor. Assume subtractor circuit input (B) range from -20 to +20. Subtractor determines how far input number is from its maximum and minimum value (error signal). Adder and D register form an accumulator. Accumulator adds the difference (error signal) to the running total (sigma). If error small, sigma change by small increment. If error large, sigma change by large increment. If sigma is positive, Most Significant Bit (MSB) goes low and feedback to delta section with maximum positive value (+20). If sigma is negative, MSB goes high and feedback to delta section with maximum negative value (-20). Bit stream is sent through 1 bit DAC and changed into analog signal. Bit stream contains average of energy represented in digital sample. One bit DAC contains of that converts the logic information (low / high or 0 / 1) to two precise analogue voltage levels, for example -1V and +1V. Analog output goes through a low pass filter that smoothes out the sudden changes and produce a smoothly changing voltage (average value of bit stream) [2]. The circuit operation can be illustrated in Figure 5.

III. PRINCIPAL OF CIRCUIT OPERATION

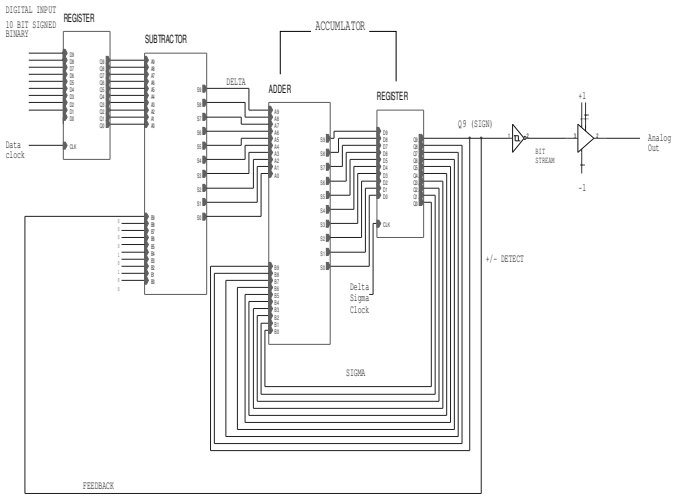

Fig. 4. Delta Sigma DAC Block Diagram

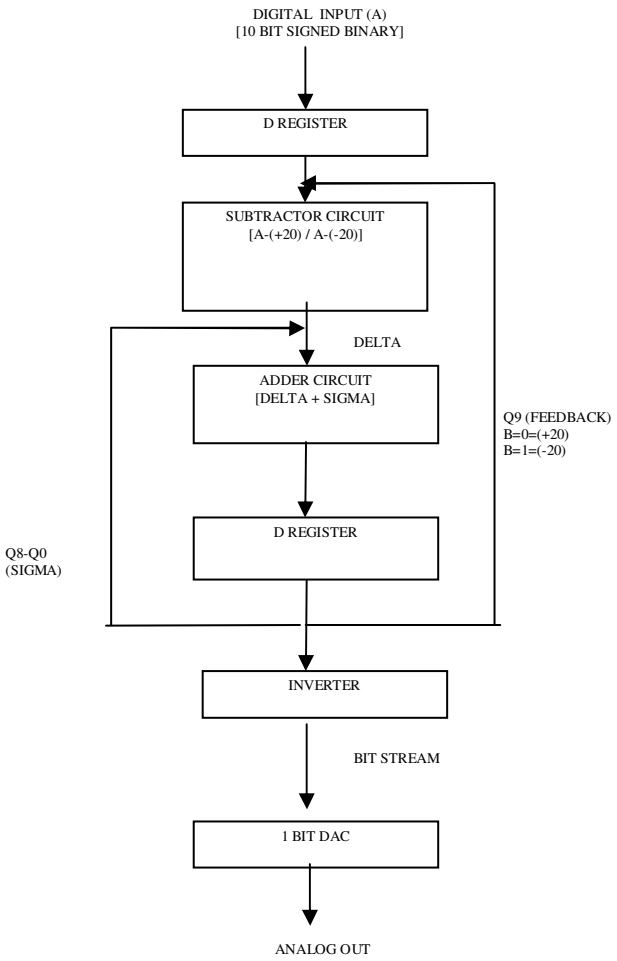

Fig. 5. Circuit Operation Flow Chart

IV. Result and Discussion

A. Calculation Result

Initially, calculations were done so that the output results of Delta Sigma DAC follow the project requirement. The desired Delta Sigma DAC voltage output is 900mV and the frequency is 4Hz. This value is chosen basically by referring to the previous research [1]. The output of 900mV is needed to be as an input voltage require by potentiostat (op-amp) which is a part of In Vivo Voltammetry System general block diagram design by another researcher. Therefore, Delta Sigma DAC Analysis as shown in Table 1 was prepared to observe the effect of any value of digital input from -20 to +20. This analysis displays the corresponding digital bit stream and analog output according to digital input. An average value of analog output is calculated to ensure the desired Delta Sigma DAC voltage output is met. The operation begins when digital input 0000010010 (18 in decimal number) is load into register. The maximum value for input is 20. The output is HIGH for 38 samples and LOW for 2 samples, a pattern that repeats every 40 samples [2].

Thus, the average value of analog output is

$$\frac{sum\ of\ analog\ input}{number\ of\ samples} = average\ voltage\ output$$

$$\frac{1+1+.....+1+(-1)+(-1)}{40} = \frac{36}{40} = 0.9\text{V} \quad (1)$$

The time scaling was taken each 0.25s due to the sampling frequency of 4Hz.

$$t = \frac{1}{f}$$
$$= \frac{1}{4Hz}$$
$$= 0.25s \quad (2)$$

TABLE I
DELTA SIGMA DAC ANALYSIS

sample (n)	Delta	Sigma	Bitstream out	Analog OUT	Feed back	AVG
0	-2	0	1	1	20	
1	38	-2	0	-1	-20	
2	-2	36	1	1	20	
3	-2	34	1	1	20	
4	-2	32	1	1	20	
5	-2	30	1	1	20	
6	-2	28	1	1	20	
7	-2	26	1	1	20	
8	-2	24	1	1	20	
9	-2	22	1	1	20	
10	-2	20	1	1	20	
11	-2	18	1	1	20	
12	-2	16	1	1	20	
13	-2	14	1	1	20	
14	-2	12	1	1	20	
15	-2	10	1	1	20	
16	-2	8	1	1	20	
17	-2	6	1	1	20	
18	-2	4	1	1	20	
19	-2	2	1	1	20	
20	-2	0	1	1	20	
21	38	-2	0	-1	-20	
22	-2	36	1	1	20	
23	-2	34	1	1	20	
24	-2	32	1	1	20	
25	-2	30	1	1	20	
26	-2	28	1	1	20	
27	-2	26	1	1	20	
28	-2	24	1	1	20	
29	-2	22	1	1	20	
30	-2	20	1	1	20	
31	-2	18	1	1	20	
32	-2	16	1	1	20	
33	-2	14	1	1	20	
34	-2	12	1	1	20	
35	-2	10	1	1	20	
36	-2	8	1	1	20	
37	-2	6	1	1	20	
38	-2	4	1	1	20	
39	-2	2	1	1	20	0.9
40	-2	0	1	1	20	0.9
41	38	-2	0	-1	-20	0.9
42	-2	36	1	1	20	0.9

B. Pspice Simulation Result

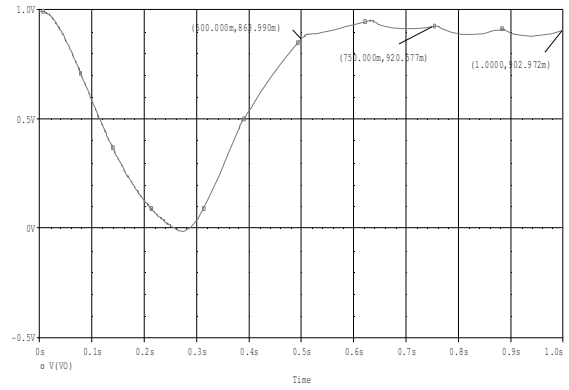

Fig. 6. Result of 900mV voltage output using PSpice Simulation

TABLE II
PSPICE RESULT

Time	PSpice	Voltage Error
500ms	863.990mV	-24.429Mv
750ms	920.577mV	-8.3722Mv
1s	902.972mV	0mV

The binary input is 0000010010 which are 18 in decimal number. This DAC is monotonic which is the voltage output increased 50mV as the binary input incremented 1 bit.

From the graph in Figure 6, the desired output which is 900mV was achieved at 1s. The voltage output is observed every 250ms or 0.25s due to sampling input at frequency of 4Hz as shown in calculation in equation (2). However, the DAC simulation has a settling time of 1s as shown in Table 2. Besides, the circuit operation takes 500ms to complete binary input sampling due to clock frequency of 4Hz D input register and the complete one cycle operation of 250ms. The voltage output has small ripples because of application Butterworth filter with Sallen-Key circuit topology. The unity-gain Sallen-Key was chosen as an analog filter because of the simplifications that Sallen-Key provide for easier selection of circuit components, and at unity gain, it has no gain sensitivity to component variations. The transient response of a Butterworth filter to a

pulse input shows moderate overshoot and ripples compared to Chebyshev filter.

This DAC implement Delta Sigma Modulator which used Pulse Density Modulation (PDM). In a pulse-density modulation bitstream of a 1 corresponds to a pulse of positive polarity (+1V) and a 0 corresponds to a pulse of negative polarity (-1V). The voltage output was obtained by averaging of 1V (bit 1) and -1V (bit 0) from bitstream over 40 samples.

The method to decode a PDM signal into analog is to pass the PDM signal through an analog low-pass filter. This method works because the function of a low-pass filter is essentially to average the signal. The average amplitude of pulses is measured by the density of those pulses over time, thus a low pass filter is the only step to reconstruct the signal.

V. Conclusion

Delta Sigma DAC has been successfully designed and simulated using PSpice simulation. The desired voltage output of 900mV at 4Hz input sampling and 50mV voltage resolution was achieved according to project specification.

VI. Future Development

The project can be further improved by reducing or eliminate ripples at voltage output. More over, the resolution of Delta Sigma DAC can be changed according to desired resolution. For example, 50mV voltage resolution can be changed to 100mV resolution by modifying the subtractor circuit feedback value to 0000001010 (10 in decimal number).

In addition, the design of analog low pass filter using Butterworth filter can be changed to Bessel filter to obtain smooth voltage output. It has constant-group delay which means that the square-wave signal is passed with minimum distortion (overshoot). In contrast, voltage output will experience a slower rate of attenuation above cutoff.

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