INTERNATIONAL JOURNAL OF UNDERGRADUATE

DESIGN AND ANALYSIS OPERATIONAL AMPLIFIER USING VLSI SOFTWARE

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ABSTRACT

This paper describes the design procedure of two stage op amp and folded cascade op amp using VLSI software. Designing high-performance analog circuits is becoming increasingly challenging with the persistent trend toward reduced supply voltages and low power consumptions but there is trade off among other performances parameter. The appropriate topology among various possible alternatives architecture of operational amplifier is selected in order to achieve higher performance for a desired application. By setting the target specification of the desired performance parameter, the value of the power supply voltage and the bias current can be determined. It start by defined the topology of the operational amplifier circuit that consist of three stage; differential amplifier, common source and output buffer. The folded cascade is then implemented to the circuit to improve the performance. The folded op amp feature high bandwidth, low supply voltage and low power dissipation. The op amps have been designed with a standard 2µm CMOS technology by using Tanner Tool. Measurement shows the unit gain bandwidth of folded op amp is 5 MHz for a 12 pF load and the amplification is 93 dB, while drawing 20 µA for 2.5 V power supply. It shows that the dc gain of folded op amp is 14 dB higher than two stage op amp and the bandwidth also 5 times larger than 2 stage op amp. The folded op amp can swing up output voltage 99% close to power supply.

Keywords: Operational Amplifier; CMOS; Gain Bandwidth, Folded Cascode, Voltage Swing.

Introduction

Operational Amplifier is an integral part of many analog and mixed-signal systems. Op amps with vastly different levels of complexity are used to realize functions ranging from dc bias generation to high speed amplification or filtering. The design of operational amplifier continue to pose a challenge as the supply voltage and transistor channel lengths scale down with each generation of CMOS technologies. In the last two decades, the design of CMOS operational amplifier especially voltage op amp, has been focus. Many efforts have been made for the reduction of both the supply voltage and the power consumed by the CMOS circuits (1). Better understanding of the characteristic and architecture of operational amplifier is essential to design the circuit. Constant aim to design low power and low voltage of analog circuit has lead to development of efficient topologies operational amplifier. By implementing folded cascade technique has improve the performance of op amp. The design start by define the stages of the circuit and selecting the current bias, current mirror, voltage supply and device sizing. The initial value is determined through the calculation before running the circuit. The requirements of this project are limited to 2.5 V voltage power supply and the power consumption is not less than 1 mW. The power consumption is the amount of quiescent power that must be consumed by the op amp in order to operate properly. The advantages of the folded op amp are it offers larger dc gain and bandwidth and better output voltage swing compare to two stage op amp. It suitable for the analog VLSI high frequency signal processing applications. This paper is set out as follows: Section II discuss the previous works, Section III explain the circuit implementation, Section IV brings the results and discussion and Section V gives the conclusion. A numbers of operational amplifier architecture exists in literature with (1) introduces novel complementary folded-cascode operational amplifier (op amps) with high gain, large bandwidth, and rail-to-rail input range for low-

voltage operation is presented by Roewer and Kleine (1) as shown in Figure 1. This op amp feature high bandwidth due to minimum internal nodes. The output swing is increased by property adjusting the output cascade transistor gate voltages close to the power supply voltages. The design of a folded cascade amplifier consists of two complimentary differential input pairs with two complementary current mirrors as active loads. The current mirrors are connected with complimentary transistors o form a class-AB cascade output stage. In general, it is designed for internal chip use only and can be redesigned to meet other requirements. The op amps have been fabricated with a standard 0.8-µm CMOS technology.

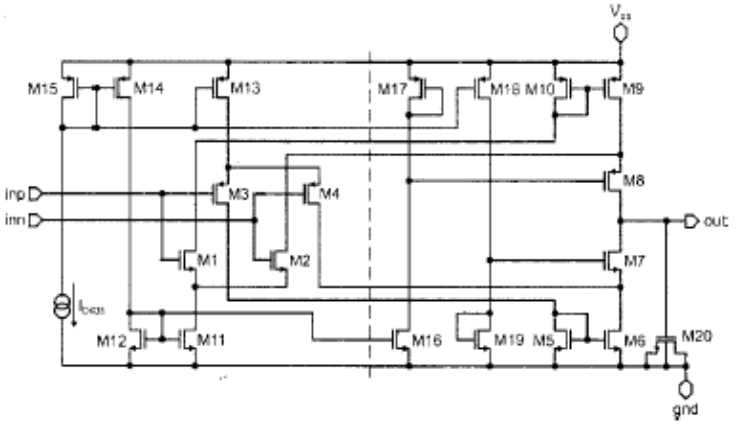

Figure 1: Novel complementary folded-cascode operational amplifier

The design procedure of the two stage CMOS operational amplifier employing Miller capacitor in conjunction with the common-gate current buffer is presented by J. Mahattanakul (2) as shown in Figure 2. The proposed procedure is based upon the design strategy that results in op amp with only one dominant pole. It proposed novel technique compensation where the smaller capacitor value can be used to compensate the circuit. The simulation of performance confirmed that the proposed design can be used to design the op amp that meets all the desired specifications.

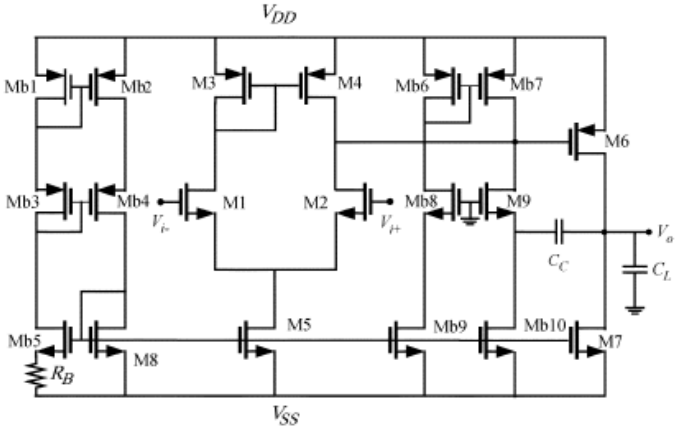

Figure 2: Op amp with robust bias circuit

Vincence (3) designed CMOS low-voltage operational amplifier, which uses a minimum selector circuit to control the class AB operation of the output stage. He emphasized on the output stage due to its high current, demanded by the resistive nature of the load. A very simple operational amplifier with class AB output is proposed. The amplifier structure is very simple, its power consumption is low, and it can operate with supply voltages down to 1.5 V. The implemented of the bias control circuit using the minimum current circuit is

proposed here. The operational amplifier basic characteristics are analyzed and simulated using the SMASH 4.0 simulator with the ACM model of the MOSFET. The design is being integrated on AMS 0.8µm CMOS technology. The paper (5) discussed the issues facing analog designers in implementing low voltage circuits and examined the possible low voltage design techniques. The techniques that become the issues are the scaling down the threshold voltage of MOSFET technique and voltage mode circuits (VMCs) approach. The first issue results in increased static power dissipation, noise and offset voltage constraints. The second issue, VMCs suffer from the drawback that the output voltage does not change instantly, low bandwidth, and not very high slew rate (SR). The possible low voltage design techniques that are examined in the paper are MOSFETs operating in the sub-threshold region, bulk-driven transistors, self- cascode structures, floating gate approach and the level techniques as shown in Figure 3. Use of low voltage high performing building blocks in low voltage analog circuits is another promising approach and yields a modular design concept in analog circuits as well. Depending upon the nature of the application, one can choose an appropriate technique or a combination of these techniques for the intended analog circuit design.

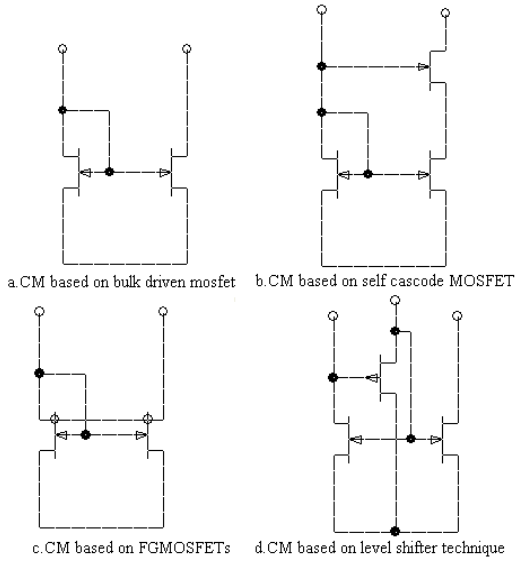

Figure 3: Analog circuit design techniques

Circuit Implementation

The CMOS operational amplifier design process consists of determining the suitable circuit, defining circuit inputs and outputs, hand calculations, circuit simulations, layout of the circuit, simulation including parasitic and reevaluation of the circuit inputs and outputs. The building block of a CMOS op amp consists of voltage reference, current mirror, current sinks, differential amplifier and output buffer. The folded cascade operational amplifier implemented has two stages; differential input stage and folded cascade load stage. While designing the operational amplifier meticulous choice of these configurations is essential for proper functioning of amplifiers.

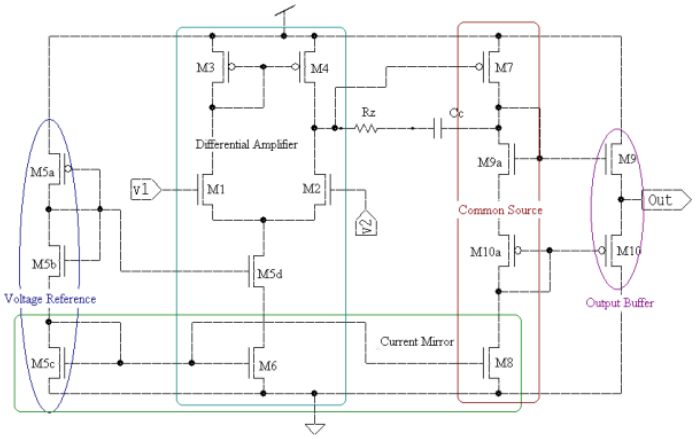

Figure 4: Two stage op amp

The reference voltage from the power supplies is derived using the resistor and the MOSFET. The MOSFET only voltage divider is chosen and implement in this project because it is has the advantage that the layout can be small. The Figure 4 shows that (M5b, M5c and M5d) generates a reference voltage equal to the voltage on the gates of the MOSFETs with respect to ground. Differential amplifier is responsible for accepting differential inputs and amplifies each of them there by passing them to the load stage regardless by its differential mode gain and its common mode gain. An important aspect of the differential amplifier is its
ability to reject a common signal applied to both inputs.

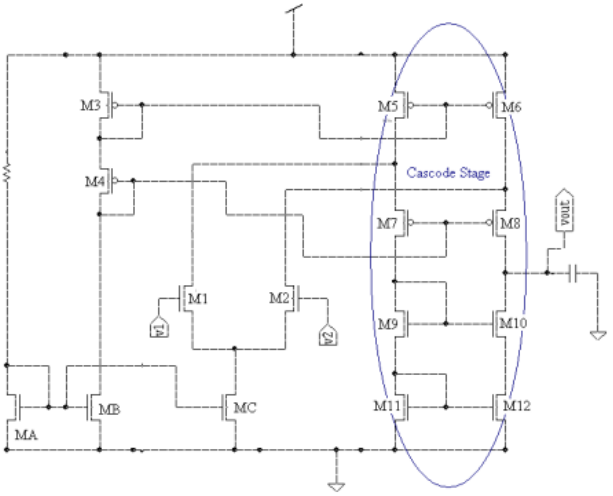

Figure 5: Folded Cascode Op Amp

Figure 5 shows the architecture of folded cascode amplifier. This stage contains 2 PMOS cascaded over 2 NMOS pairs. It provides the required load and output resistance for the output stage. High output resistance of this stage would yield high gain from this stage. The configuration that provides low gain-high swing and low power cascade stage would be implemented in the design.

RESULTS AND DISCUSSION

The proposed circuit was designed using TANNER Tool for both schematic and layout. It was implemented in 2.0 µm process with 2.5 V power supply and simulated with T-Spice.

The performance summary of two operational amplifiers is summarized in Table I and the final layout of the operational amplifier is depicted in Figure 7. The area of the core layout is about 3.7187×10^{6} μm^{2} with power consumption about 1 mW. The AC simulation results are shown in Figure 8 showing that the DC gain is 93 dB and the bandwidth is 5 MHz with phase margin about 93 degree.

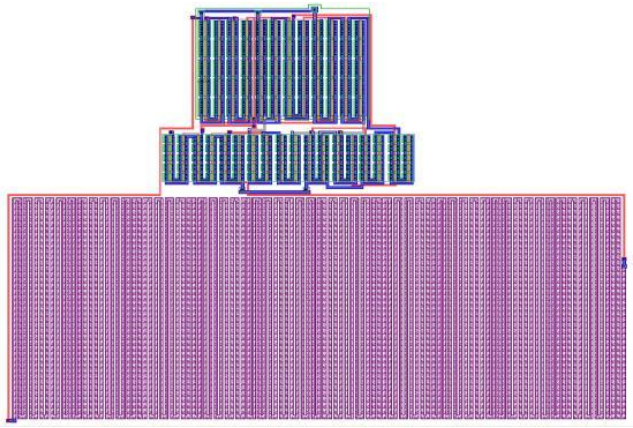

Figure 7: Layout of folded op amp

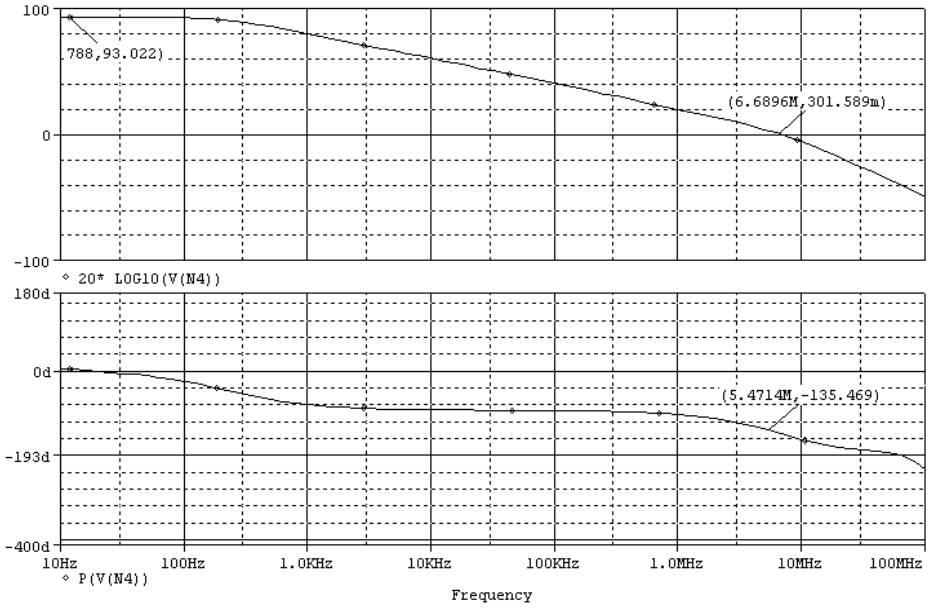

Figure 8: Open loop frequency response of folded op amp

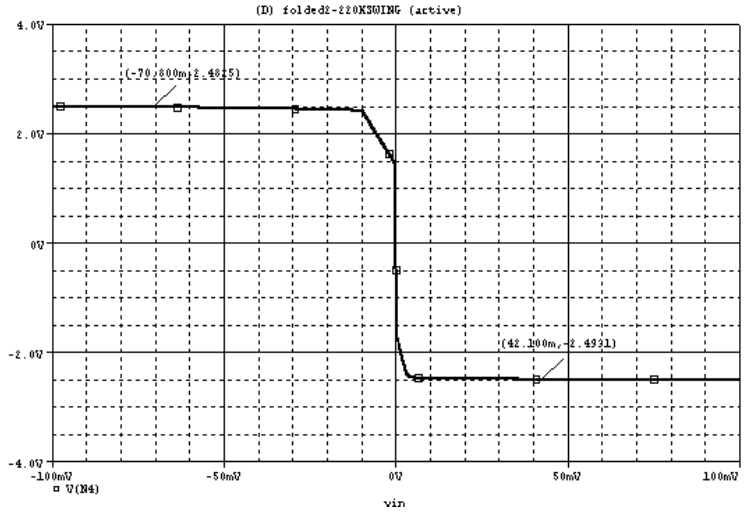

Figure 9: Voltage Swing of Folded Op Amp

The voltage swing indicates the value of positive or negative saturation of the op amp. The output voltages never exceed these limitations for supply voltages V_{DD} and V_{SS}. The folded cascade has the major advantage compare the basic operational amplifier where it can swing up 99% close to the V_{DD} and V_{SS}. The simulation in Figure 9 shows the maximum output voltage swing is +2.49 V and the minimum output voltage swing is -2.49 V.

□

Table I: Comparison Results

Folded Cascode Operational Amplifier			
Technology		2.0 µm CMOS N-well process	0.8 µm CMOS Technology[2]
Supply Voltage	(V)	V_{DD} = +2.5 V_{SS} = -2.5	V_{DD} = +5, V_{SS} = -5
Load Capacitor, C_L	(pF)	12	5
Differential Gain A_{VO}	(V/V)	93 dB	81.5
Differential GBW	(MHz)	5.47	20.5
Phase Margin	(°)	45	68.5
Power Dissipation	(mW)	0.44	3.9
CMRR	(V/V)	96 dB	60
Slew Rate	(V/µs)	2	5.8
Output Voltage Swing	(V)	Max = +2.49 Min = -2.49	Max = +4.3 Min = +0.7
Input Offset Voltage	(mV)	0.025	5.6
Area	□m^2	3.7187□10^6	143

CONCLUSION

The folded cascade operational amplifier provide low voltage power supply, high bandwidth and low power dissipation compare to the two stage operational amplifier. It is widely used in used in VLSI chips because the performance can be tailored to the specific application easily. Simulation results confirm that folded cascade op amp has larger dc gain than 2 stage op amp. The bandwidth also increased about 5 times larger than 2 stage op amp about 5 MHz which is suitable for analog VLSI high frequency signal processing applications. The output voltage swing is 99% close to power supply and the power dissipation is reduced 50% than targeted value. The circuit consumes a large area in the layout due to the bigger size of the MOSFETs. In term of size of layout, it is not practical because it consumes larger area. The maximum current that can be driven by the circuit is 20 mA and it is not enough of driving heavy resistive and capacitive loads. The presented circuit can be redesigned with other different technology to meet other requirement. The presented structure can be easily designed to meet other requirement and applications. The improvement of the performance can be made by implementing the complementary folded cascade architecture for high frequency and it consumes small area in the layout. The presented circuit can also be designed with other different technology such as 0.35 μm technology which is smaller and gives the better performance. The voltage reference technique can be used to replace the resistor.

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