ELECTRICAL ANALYSIS OF SI_3N_4 CAPPING LAYER AND SOI TECHNOLOGY IN SUB-65 nm CMOS

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ABSTRACT

Starting at the 65nm node, stress engineering to improve performance of transistors has been a major industry focus. An intrinsic stress source, shallow trench isolation (STI) has not been fully utilized up to now for circuit performance improvement. In this paper, two methods have been used on 65nm CMOS that combines with detailed placement and active-layer fill insertion to analyze for performance improvement.

First method is to investigate electrical characteristics for 65 nm NMOS by using Si_3N_4 capping layer for three different layers thickness (30 nm, 60 nm and 100 nm. Second method is using 0.4 μm thickness of Silicon-on-Insulator (SOI) Technology for 65 nm PMOS. The performance of the devices is analyzed by focusing on the electrical characteristics of Id– Vd and Id–Vg curves for both capping layer and SOI technology.

The results shows that, thicker capping layer thickness offer higher stress in CMOS, this improves the acceleration of electron mobility and increases the drive saturation current in NMOS of about 14%. Meanwhile, by implemented SOI technology shows improvement in threshold voltage (with decrement of 8.5%) and drain saturation current (with increment of 4.7%). The fabrication process simulation and electrical characteristic was simulated by using SILVACO TCAD ATHENA and ATLAS simulator.

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CHAPTER 1

INTRODUCTION

1.0 Chapter Overview

This chapter describes the objective of this project, brief explanation process involved, scope of work that have been done in completing this project and overall chapter in this project.

1.1 Background

CMOS are becoming very popular devices nowadays. The widely used CMOS has forced the industries to compete among themselves in order to produce the best performance of CMOS. The technologies and demands have caused the reducing on the gate length of the CMOS from 130nm to 65nm. Recently, industries have begun shipping products built on 65nm technology.

Device structure and fabrication play an important role in determining the overall effectiveness, performance, and cost of a logic chip. Logic devices are attaining smaller process geometries and higher levels of integration. 65nm processes offer designers the capability to integrate more complex functionality at higher performance on a single chip. However, the smaller geometry gates do not come without a cost, and an increasingly dominant one is power dissipation [14].

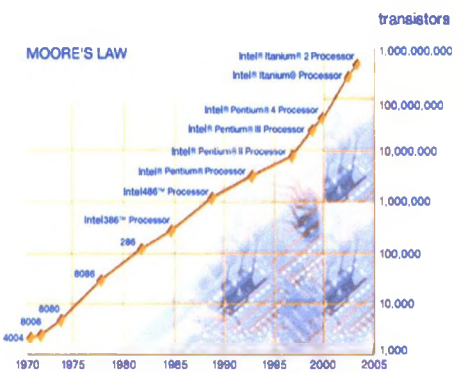

Figure 1.1 Moore's Law