# ELECTRICAL PROPERTIES AND MORPHOLOGY MICROSCOPY OF PALLADIUM (Pd) SCHOTTKY CONTACT ON P-TYPE GaN

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*Abstract*: In this paper, we present the electrical, thermal, and morphological characteristics of Pd contacts to Mg-doped p-type GaN grown on sapphire substrate. Different annealing temperatures (300-700°C) were investigated, as thermally stable metal-semiconductor contacts are essential for high quality devices. The barrier heights and leakage current of these contacts determined using current-voltage (I-V) measurement were investigated. The surface morphology of the samples were assessed by Scanning Electron Microscopy (SEM) in which the change of structural property could significantly affect the performance of contacts. The experimental result revealed that the sample annealed at 400°C for 35 minutes was the optimum condition where the highest SBH (0.68 eV) with low leakage current (20  $\mu$ A at -5V) was obtained.

Keywords: Leakage current, Schottky barrier height, Schottky contact, Thermal annealing

## INTRODUCTION

GaN and related III-V nitrides semiconductors are the focus of intensive research due to their superior properties such as wide direct band gap, large breakdown field, high electron velocity, and high chemical stability at elevated temperature which make them suitable for high frequency, high power electronic devices such as field effect transistors (FETs), high electron mobility transistors (HEMTs), power rectifiers and UV detectors [1]. Furthermore, in the GaN-based metal semiconductor field effect transistor (MESFET) device, thermal stability of the Schottky diode [2,3] is one of the key issues.

The fabrication of high-quality contacts with thermal stability and reliability is of technological importance for device performances. The optimization of the performance of these devices would require high quality or intimate metal-semiconductor contacts, where this has prompted many extensive researches in developing high quality low resistance ohmic contacts. It is very difficult to measure Schottky barrier height of p-GaN contacts using conventional current-voltage (I-V) methods due to the lack of low-resistance ohmic contact. As a result, very limited information on the barrier heights and acceptor concentrations obtained by the conventional I-V is available in the open literature [3]. In this work we report the study of current-voltage (I-V) and leakage current characteristic in p-type GaN Schottky diodes as a function of annealing.

## MATERIALS AND METHODS

Mg-doped p-GaN samples grown on sapphire (Al<sub>2</sub>O<sub>3</sub>) substrates were used. The carrier concentration of the samples is about  $10^{17}$ - $10^{18}$  cm<sup>-3</sup>. The ohmic metallization consists of a bi-layer of Ni/Ag, and Pd as a Schottky contacts, were treated under different annealing temperatures and durations. Prior to the metallization, the native oxide was removed with NH<sub>4</sub>OH : H<sub>2</sub>O=1:20 solution, followed by dipping in a HF:H<sub>2</sub>O=1:50 solution. Boiling aqua regia (HCl:HNO<sub>3</sub> = 3:1) was used to chemically etch and clean the samples.

Two stripes of bi-layer of Ni/Ag were first formed on p-GaN to act as ohmic contacts. The Ni/Ag bilayer contacts were checked and confirmed to be ohmic by I-V measurement prior to the deposition of Pd Schottky contact. Pd metallized dots with a diameter of 250  $\mu$ m for Schottky contacts were evaporated via a metal mask onto the p-GaN samples. The top and cross section view of the ohmic and Schottky contacts of a typical sample are shown in Figure 1.

Three sets of current-voltage (I-V) measurements were obtained in this study. The samples were annealed under flowing nitrogen gas environment in the furnace ranging from 300°C to 700°C for three

different annealing durations, i.e. 5, 15 and 35 minutes. The I-V characteristics of Pd diodes under different conditions were measured by keithley High-voltage-source-measure-unit model 237 semiconductor parameter analyzer.



Figure 1: (a) Top view, and (b) cross section view of ohmic and Schottky contacts of a typical sample

# **RESULTS AND DISCUSSIONS**

The electrical parameters, i.e., Schottky barrier heights,  $\Phi_B$ , saturation current,  $I_{\omega}$  and ideality factor,  $\eta$  can be determined by I-V measurements. For thermionic emission and V>3kT/q, the general diode equations are [4]:

$I = I_o \exp\{qV/(\eta kT)\}$	(1)
$I_o = AA * T^2 \exp\{-q \Phi_B / (kT)\}$	(2)

As usual, A is the contact area, k is the Boltzmann's constant, T is the absolute temperature,  $\Phi_B$  is the barrier height and  $A^*$  is the effective Richardson coefficient. The theoretical value of  $A^*$  can be calculated using  $A^{*}=4\pi m^*qk^2/h^3$ , where h is Planck's constant and  $m^*=0.80m_o$  is the effective hole mass for GaN [12]. The value of  $A^*$  is determined to be  $103.8 \, A \, cm^2 K^2$ . The plot of Ln I vs V will give a straight line with a slope of  $q/(\eta kT)$ , and the intercept with y-axis will yield  $I_o$ , in which barrier height,  $\Phi_B$  can be obtained using Equation (2).



Figure 2: Ln I vs V of the Pd/p-GaN Schottky diodes at different annealing temperatures for 35 minutes

Figure 2 shows Ln I versus V of Pd Schottky contacts on p-GaN annealed at various temperatures for 35 minutes. From the curves, sample annealed at 400°C has the lowest saturation current,  $I_{o}$  which was deduced to be  $1.81 \times 10^{-8}$ A. On the other hand, highest  $I_{o}$   $1.78 \times 10^{-6}$  A was obtained for the sample annealed at 300°C. The ideality factor,  $\eta$ , determined from the curves, was found to be much greater than unity, this indicates that a significant amount of the current could be due to other current transport mechanisms rather than thermionic emission model. An ideality factor,  $\eta > 1$  could be ascribed to interface states at a thin oxide between the metal and semiconductor [5], or generation-recombination currents within the space region [6].

The SBHs of Pd Schottky diodes annealed at various temperatures for different durations were calculated and listed in Table 1. The data reveal that thermal treatment could affect the electrical properties of the Schottky diodes significantly. The samples with the highest SBHs for three different annealing durations, i.e. 5,15, and 35 minutes are coincidently found to be annealed at 400°C, however, further increase of the annealing temperature will lead to the decrease of the SBHs. The annealing duration of 15 minutes has little impact on the SBHs, a slight increase of the SBHs is found compared to 5 minutes of annealing. However, for 5 minutes as opposed to 35 minutes annealing duration, a significant increase of the SBHs was observed for annealing temperatures between 300 to 500°C. The increase of the SBHs could be attributed to the prolonged annealing duration. The presence of small amount of oxygen during annealing could cause the formation of a oxide layer under a prolonged annealing times, the samples become more of metal-insulator-semiconductor type structure [7]. Schottky barrier height at the metal/semiconductor interface is the result of several competitive processes including the metal work function, interface states due to defects, reaction of the products and states that are induced by metal deposition [8]. Therefore the decrease of the barrier height for the further increase of the annealing temperatures (>400°C) could be due to the change of interface states.

Annealing temperature	Annealing 5min		Annealing 15min		Annealing 35min	
	SBH , $\Phi$ (eV)	LC,( mA ) at -5V	$SBH, \Phi$ (eV)	LC,( mA ) at -5V	$SBH, \phi$ (eV)	LC,( mA ) at -5V
As-deposited	*0.51	*2.460	-	-	-	-
300°C	0.52	0.835	0.53	0.145	0.56	0.214
400°C	0.62	0.069	0.63	0.017	0.68	0.020
500°C	0.61	0.086	0.62	0.047	0.64	0.038
600°C	0.58	0.100	0.59	0.060	0.59	0.047
700°C	0.57	0.300	0.58	0.105	0.57	0.220

Table 1: The comparison of SBH and LC of Pd Schottky contact for various annealing temperatures and duration.

LC ( Leakage current ), SBH ( Schottky Barrier height ), \* without heat treatment

Figure 3 illustrates the reverse I-V characteristics of Pd/p-GaN annealed at different temperatures for 35 minutes. Before heat treatment, leakage current (LC) was substantially found in Pd contacts. After annealing process, the leakage current was reduced significantly. Table 1, shows the leakage current of the Pd diodes at various temperature under different annealing times. Generally, the lowest LCs were also observed at 400°C for three different annealing durations, and it increased gradually with the annealing temperatures. The annealing durations was found to have a impact on the LC.

Figure 4 reveals that the optimum annealing time was 15 minutes, further annealing would increase the LC. The LC gradually decreased as the annealing temperature increased to 400°C, this could be attributed to the removal of defects from the material and subsequent improvement of the quality of ohmic contact [9]. However further increase of the annealing temperature, the leakage current began to increase, this could be due to the degradation of both the GaN and ohmic contact after high temperature annealing. It is interesting to note that the lowest LCs are observed to be matched with the highest SBHs for three different annealing times, (i.e. 5, 15, 35 minutes). Similar findings were also reported

Tan Chee Kiat et al.

[10]. It is highly desirable to get a large Schottky barrier height for rectifying metal contacts on GaN with low leakage [11].



Figure 3: The reverse I-V characteristics of Pd/p-GaN annealed at various temperatures for 35 minutes







(e) Annealed at 600°C





Figure 5 illustrates the SEM images for the samples annealed at different temperature for 35 minutes annealing duration. The as-deposited and annealed samples ( $<500^{\circ}$ C) showed no significant change of surface morphology. However, rough surfaces were observed for samples annealed at 500°C, more obvious at 600°C and became even grainy for further annealing at 700°C. This could be due to the increase of annealing temperature and, caused degradation of both GaN and the ohmic contact eventually. This might lead to the increase of leakage current or the decrease of SBHs at metal/p-GaN interface in I-V measurements for Pd Schottky diodes.

## CONCLUSION

The SBHs and LCs were found to be sensitive to the change of annealing temperature and duration. Annealing at temperature of 400°C were coincidently produced the optimum SBHs as well as for leakage current for different annealing duration, due to the improvement of material and ohmic contact. Upon annealing at 700°C, the reverse diode characteristics were significantly degraded where it may be attributable to the formation of metal-insulator-semiconductor type structure. Changes in the surface morphology of the contacts upon annealing were also examined. Metal island formation was observed at high annealing temperatures.

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#### REFERENCES

- 1. Koyama, Y., Hashizume, T., Hasegawa, H. 1999. Solid-State Electronics. 43:1483
- 2. Liu, Q. Z. and Lau, S. S. 1998. Solid-State Electronics. 42:677.
- 3. Wang, C. W., Liao, J. Y., Chen, C. L., Lin, W. K., Su, Y. K. and Yokoyama. 1999. M. Journal of vac. Sci. Tech. 28:341.
- 4. Sze, S. M.1989. Physics of Semiconductor Devices, 2<sup>nd</sup> edition, John Wiley & Sons, New York.
- 5. Werner, J. H., Levi, A. F. J., Tung, R. T., Anzlower, M. and Pinto, M.1988. Phys. Rev. Lett. 60 :53
- Rhoderick, E. H. and Williams, R. H. Metal-Semiconductor Contacts. Clarendon Press. Oxford. 2<sup>nd</sup> edition. ch. 3:118
- 7. Chen, G. L., Chang, F. C., Shen, K.C. Ou, J., Chen, W. H., Lee, M. C., Jou, M. J. and Huang, C. N. 2002. Applied Physics letters. 80: 4
- 8. Wu, C. I., Kahn, A. and Vac, J. 1998. Sci. Technol. B. 16: 2218
- 9. Lee, K. N., Cao, X. A., Abernathy, C. R., Pearton, S. J., Zhang, A. P., Ren, F., Hickman, R. and Van Hove, J. M. 2000. Solid State Electronics. 44 :1203-1208
- 10. Miura, N., Nanjo, T., Suita, M., Oishi, T., Abe, Y., Ozeki, T., Ishikawa, H., Egawa, T. and Jimbo, T. 2004. Solid-State Electronics. 48: 689-695
- 11. Suzue, K., Mohammad, S. N., Fan, Z. F., Kim, W., Aktas, O., Botchkarev, A. E. and Morkov, H. 1996. Journal of Appl. Phys. 80:4467
- 12. D. Donoval, V. Kulikov, P. Beňo, J. Racko. ASDAM 2002.