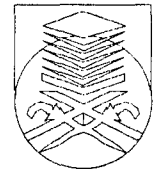
# DEVELOPMENT AND ANALYSIS OF Si/SiGe BASED CMOS



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By:

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NOVEMBER 2005

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Tarikh : 4 Mac 2004
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Pn. Nurulhuda Abd Rasheid
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Puan,

**TAJUK PROJEK: 'DEVELOPMENT AND ANALYSIS OF Si/SiGe BASED CMOS'**

Dengan hormatnya perkara di atas adalah dirujuk.

Sukacita dimaklumkan bahawa Jawatankuasa Penyelidikan dan Perundingan di peringkat Fakulti telah membuat keputusan:

i. Bersetuju meluluskan cadangan penyelidikan yang dikemukakan oleh puan serta Pn. Zaiton bt Sharif dan Pn. Zuriati bt. Janin.

ii. Tempoh projek penyelidikan ini ialah 12 bulan, iaitu mulai **1 hb Mac 2004** hingga **28 hb Februari 2005.**

iii. Kos yang diluluskan ialah sebanyak **RM20,000.00** sahaja.

iv. Penggunaan geran yang diluluskan hanya akan diproses setelah perjanjian ditandatangani.

v. Semua pembelian peralatan yang kosnya melebihi RM500.00 satu item perlu menggunakan Pesanan jabatan Universiti Teknologi MARA (LO). Pihak tuan juga dikehendaki mematuhi peraturan penerimaan peralatan. Panduan penerimaan peralatan baru dan pengurusannya dilampirkan bersama.

vi. Kertaskerja boleh dibentangkan di seminar setelah **75% deraf awal laporan akhir projek** dihantar ke Biro untuk semakan. Walau bagaimana pun, tuan perlu membuat permohonan kepada Biro Penyelidikan dan Perundingan.


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: 03-55435107
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Tarikh : 30 November 2005
No. Fail Projek : 600-IRDC/ST.5/3/699

Penolong Naib Canselor (Penyelidikan)
Institut Penyelidikan, Pembangunan dan Pengkomersilan (IRDC)
UiTM, Shah Alam

YBhg. Prof.,

**LAPORAN AKHIR PENYELIDIKAN "DEVELOPMENT AND ANALYSIS OF Si/SiGe BASED CMOS"**

Merujuk kepada perkara di atas, bersama-sama ini disertakan 2 (dua) naskah Laporan Akhir Penyelidikan bertajuk "Development And Analysis of Si/SiGe Based CMOS".

Sekian, terima kasih.

Yang Benar,

**NORULHUDA ABD RASHEID**
Ketua
Projek Penyelidikan

# ABSTRACT

Complementary metal-oxide-semiconductor (CMOS) is currently the most dominant technology used in making integrated systems. It consists of both n-channel MOS transistor (NMOS) and p-channel MOS transistor (PMOS) fabricated on the same substrate. Conventionally, the substrate is made of silicon. Alternatively, the substrate can be made from different layer of semiconductors known as heterostructure. Much attention has been given to Si/SiGe due to its compatibility with silicon and higher carrier mobilities. SiGe is an alloy which is said to be an alternative solution to the problem of a down-scaled CMOS to produce high speed device.

This work consists of modelling three different of Si/SiGe heterostructure substrates which are used to construct n- and p-channel MOSFETs and later to construct CMOS inverter. The three types of heterostructures are a strained SiGe on silicon substrate, a strained silicon on relaxed SiGe/Si substrate and a strained SiGe on strained Si/relaxed layers of SiGe/Si substrate.

A device simulator, SILVACO TCAD Tools is used in this project. Although it has heterojunction capability, it does not support model for a strained Si. This work also highlights the method to simulate Si/SiGe heterostructures containing strained layer using SILVACO. Simulations on the band structure and current-voltage (I-V) characteristics of the MOSFETs are carried out. The $I_d$-$V_g$ and $I_d$-$V_d$ are simulated for different value of Ge% and mobility. This is to observe the effect of varying the value of Ge% and mobility used in the design. The simulation on the CMOS inverter as the fundamental circuit is carried out to obtain the transfer curve. The noise margin and switching characteristics can be extracted from the transfer curve.

All the simulated results are then compared with the Si bulk. The analyses show that the performance of the Si/SiGe heterostructures is better in terms of the electrical characteristics of the MOSFETs and the switching characteristics of the CMOS inverter, as compared to the performance of the Si bulk.

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