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FINAL REPORT OF DIPLOMA PROJECT

ELECTRONIC JAM

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ABSTRACT

We are developing an Electronic Jam circuit. This jam circuit can be used in quiz contests wherein any participant who pressed his button or switch before the other contestants, get the first chance to answer a question. There have a limit where only 8 contestants maximum can participated or 1-8 participants recommended not more than that. The display will show the number of the contestant who pressing his/ her button before the others from the description of the game, several the major subsystems are needed where one-digit on display for the rolling digit and the pay off, the display will show the contestant who pressed his button. At the same time, the buzzer will also sound.

Nowadays, quiz contest become popular such we seen it from electronic media. In developing this project, we have to improving our technique to show the necessary output to prove the function of it. This project does not have much problem to make because only used simple electronic device. The techniques for this project are not very complex, all basic components are easy to find and very cheap cost.

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CHAPTER 1

INTRODUCTION

1.1 Background

This jam circuit can be used in quiz contests wherein any participant who presses his button (switch) before the other contestants, gets the first chance to answer a question. The circuit given here permits up to eight contestants with each one allotted a distinct number (1 to 8). The display will show the number of the contestant pressing his button before the others. Simultaneously, a buzzer will also sound. Both, the displays as well as the buzzer have to be reset manually using a common reset switch. Initially, when reset switch S9 is momentarily pressed and released, all outputs of 74LS373 (IC1) transparent latch go 'high' since all the input data lines are returned to Vcc via resistors R1 through R8. All eight outputs of IC1 are connected to inputs of priority encoder 74LS147 (IC2) as well as 8-input NAND gate 74LS30 (IC3). The output of IC3 thus becomes logic 0 which, after inversion by NAND gate N2, is applied to latch-enable pin 11 of IC1. With all input pins of IC2 being logic 1, its BCD output is 0000, which is applied to 7-segment decoder/driver 74LS47 (IC6) after inversion by hex inverter gates inside 74LS04 (IC5). Thus, on reset the display shows 0. When any one of the push-to-on switches—S1 through S8—is pressed, the corresponding output line of IC1 is latched at logic 0 level and the display indicates the number associated with the specific switch. At the same time, output pin 8 of IC3 becomes high, which causes outputs of both gates N1 and N2 to go to logic 0 states. Logic 0 output of gate N2 inhibits IC1, and thus pressing of any other switch \$1 through \$8 has no effect. Thus, the contestant who presses his switch first, jams the display to show only his number. In the unlikely event of simultaneous pressing (within few nano-seconds difference) of more than one switch, the higher priority number (switch no.) will be displayed. Simultaneously, the logic 0 output of gate N1 drives the buzzer via pnp transistor BC158 (T1). The buzzer as well the display can be reset (to show 0) by momentary pressing of reset switch S9 so that next round may start.

The original circuit sent by the author has been modified as it did not jam the display, and a higher number switch (higher priority), even when pressed later, was able to change the displayed number.