ENHANCING SUBMICRON CMOS DEVICE PERFORMANCE

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ABSTRACT

Semiconductor revolution has been possible with the downsizing or scaling the size of semiconductor devices such as Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET). Scaling of MOSFET becomes very important in Ultra Large-Scale Integration (ULSI) for high integration and high speed operation. In this dissertation, a study has been done for development of 0.13μm CMOS technology. The device design, fabrication process and characterization have been discussed. By using the scaling rules, a Complementary Metal Oxide Semiconductor (CMOS) transistor with channel size of 0.13μm has been scaled down from a CMOS transistor with channel size of 0.18μm that had been designed and fabricated before. In order to achieve the desire electrical characteristic of 0.13μm CMOS transistor, several parameters have to be scaled such as channel gate length, gate oxide thickness, ion implantation for threshold voltage adjustment and other related specifications. Scaling limiting factors such as short channel effect and hot electron effect have been given much consideration by implementing lightly doped drain (LDD) structure and shallow junction of drain/source. Shallow Trench Isolation (STI) has been proposed for the isolation technique to eliminate the oxidation encroachment or bird's beak by Local Oxidation of Silicon (LOCOS). Silicide using cobalt silicide has been implemented to reduce the sheet resistance and the double metal gate for better performance. The stress analysis between the STI and LOCOS isolation technique has been done and LOCOS structure introduce more stress if compare to the STI structure.

Fabrication and simulation of the CMOS transistor is done by using Virtual Wafer Fabrication (VWF) Silvaco TCAD Tools. NMOS and PMOS were simulated individually to simplify the fabrication process and shorten the simulation time. From the simulation results, the threshold voltage for nMOS and pMOS are 0.359863V and -0.335567V respectively. As to define the functionality of 0.13μm CMOS transistor, the relation of $I_d - V_d$ and $I_d - V_g$ are presented.