UNIVERSITI TEKNOLOGI MARA
CAWANGAN PULAU PINANG

STUDY ON THE EFFECT OF SHORT GATE LENGTH ON 65NM NMOS TRANSISTOR USING SILVACO TCAD

AZIRA BINTI AHMAD TARMIZI

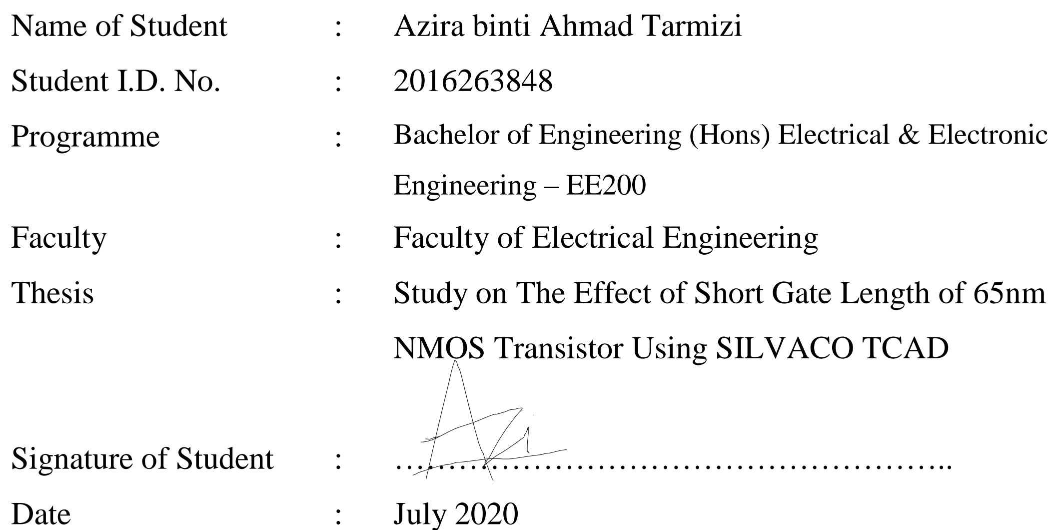
BACHELOR OF ENGINEERING (HONS) ELECTRICAL AND ELECTRONIC ENGINEERING

July 2020

AUTHOR'S DECLARATION

I declare that the work in this thesis was carried out in accordance with the regulations of Universiti Teknologi MARA. It is original and is the results of my own work, unless otherwise indicated or acknowledged as referenced work.

I, hereby, acknowledge that I have been supplied with the Academic Rules and Regulations, Universiti Teknologi MARA, regulating the conduct of my study and research.



Name of Student	:	Azira binti Ahmad Tarmizi
Student I.D. No.	:	2016263848
Programme	:	Bachelor of Engineering (Hons) Electrical & Electronic Engineering – EE200
Faculty	:	Faculty of Electrical Engineering
Thesis	:	Study on The Effect of Short Gate Length of 65nm NMOS Transistor Using SILVACO TCAD
Signature of Student	:	…………………………………………………..
Date	:	July 2020

ABSTRACT

The aim of this work is to design and study on the effect of short gate length of 65nm NMOS transistor using SILVACO TCAD. A 65nm NMOS was designed and fabricated to study its electrical characteristics. To simulate the electrical performances of the 65nm NMOS, ATHENA and ATLAS of SILVACO TCAD tools were used. Downscaling of NMOS transistors will change its operational characteristics. A shorter gate length will lead to Short Channel Effect (SCE) to arise which are channel length modulation and Drain Induced Barrier Lowering (DIBL). The Short Channel Effect can be observed from the comparison of the simulation result of the long gate length (0.3 μm) and short gate length (65nm). Based on the result, SCE which are channel length modulation and DIBL can be observed from the short gate length (65nm) NMOS transistor. The results showed that inclusion of Halo implantation has reduced the DIBL effect as the I_D plot showed that when I_D= 0 and V_{TH}= 1.87V. In addition, retrograde well doping reduced the channel length modulation since I_D increase by a factor of 1.3 which is lower compared to I_D for 65nm conventional NMOS increase by a factor of 1.6. Lastly, the Halo implantation and retrograde well have been proven to reduce the channel length modulation as well as DIBL effect shown by the findings and supported by other studies.
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// ACKNOWLEDGEMENT

Upon the completion of my project which would not have been possible without the guidance and support from certain people. I really appreciate all the contribution in both aspects mentally and physically.

First and foremost, I would like to thank God Almighty for giving me strength and patience to finish this work.

I also wish to acknowledge the support and guidance given by my supervisor, Dr. Alhan Farhanah binti Abd Rahim. All the advices and directions have been the most important factors that push me to successfully complete this project.

Finally, I should not forget to thank all my friends that have been indirectly support both mentally and technically. Their love and encouragement are the comfort I needed to ease the pressure and tension.

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