UNIVERSITI TEKNOLOGI MARA

PZT MMIC VIA HOLE FABRICATION TECHNIQUE

RAUDAH BINTI ABU BAKAR

Thesis submitted in fulfilment of the requirements for the degree of Master of Science

Faculty of Electrical Engineering

February 2010

Candidate's Declaration

I declare that the work in this thesis was carried out in accordance with the regulations of Universiti Teknologi MARA. It is original and is the result of my own work, unless otherwise indicated or acknowledged as referenced work. This thesis has not been submitted to any other academic institution or non-academic institution for any other degree or qualification.

In the event that my thesis be found to violate the conditions mentioned above, I voluntarily waive the right of conferment of my degree and agree to be subjected to the disciplinary rules and regulations of University Teknologi MARA.

Name of Candidate	:	Raudah Binti Abu Bakar
Candidate's ID No.	:	2005103093
Programme	:	MSc in Electrical Engineering (EE780)
Faculty	:	Faculty of Electrical Engineering
Thesis Title	:	PZT MMIC Via Hole Fabrication Technique

Signature of Candidate Date

ABSTRACT

This study is carried out in order to investigate the effects of via hole grounding in newly proposed high dielectric constant material, lead zirconate titanate (PZT) thin films for MMIC applications. To predict the performance of via hole in PZT thin films, $50 \times 50 \ \mu\text{m}^2$ square and cylindrical vias of various diameters were simulated using *CST Microwave Studio* over 0.1 to 20 GHz frequency range. The via test structures were patterned using a combination of electron beam lithography and wet etching technique for on-wafer characterization and were metallized with sputtered gold. The on-wafer characterization was performed using a *Wiltron 37269A* vector network analyzer and *Cascade Microtech* probe station with *Cascade Infinity* probes. The values of the resistance and inductance extracted from the simulation and measurement data were compared. The measured results exhibit inductive behaviour which is similar to those obtained from the simulation, indicating successful via realization using a new wet etching technique with 0.5HF : 5HCl : $10NH_4Cl : 50H_2O$ composition. However, the inductance (18.839 pH) and resistance (1.212 Ω) are found to be higher than the simulated values.

TABLE OF CONTENTS

TITLE	i
CANDIDATE'S DECLARATION	ii
ABSTRACT	iii
ACKNOWLEDGEMENTS	iv
TABLE OF CONTENTS	v
LIST OF TABLES	viii
LIST OF FIGURES	ix
LIST OF PLATES	xiii
LIST OF ABBREVIATIONS	xiv
LIST OF SYMBOLS	xvii

GENE	RAL INTRODUCTION	1
СНАР	TER 1: INTRODUCTION	3
1.0	Introduction	3
1.1	Monolithic Microwave Integrated Circuits and Dielectric	
	Materials Issues	3
1.2	Ferroelectric Materials for Microwave Capacitor Applications	8
1.3	PZT Thin Films	9
1.4	Low Inductance Ground Plane	16
1.5	Via Hole Fabrication Process	19
	1.5.1 Lithography	19
	1.5.2 PZT Etching	24
	1.5.3 Metallization	26
	1.5.4 Lift-off Process	27
1.6	Summary	28

CHAPTER 2: 3D SIMULATION OF VIA HOLE GROUNDING		30
2.0	Introduction	30
2.1	Via Hole Simulation Process	30
2.2	Via Hole Performance at Microwave Frequencies	35
2.3	Geometrical Effects on the Via Performance	39
2.4	Summary	46

CHAP	TER 3: FABRICATION OF VIA HOLE GROUNDING	47
3.0	Introduction	47
3.1	Via Hole Fabrication Process	47
3.2	Sample Cleaning and Resist Coating	49
3.3	Electron Beam Lithography	52
	3.3.1 Electron Beam Lithography Issues	56
3.4	PZT Etching	66
3.5	Metallization and Lift-off Process	72
3.6	Summary	74

CHAPTER 4: ON-WAFER MICROWAVE MEASUREMENT AND CHARACTERIZATION

4.0	Introduction	75
4.1	Microwave Measurement Techniques	75
4.2	On-Wafer Probe Measurement	76
	4.2.1 On-Wafer Probing	79
	4.2.2 On-Wafer Calibration	81
4.3	Via Hole On-Wafer Characterization	83
4.4	Comparison Between Measurement and Simulation	87
4.5	Summary	89

75