Gain Enhancement of Microstrip Patch Antenna

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Abstract— **In this paper , a 2x1 microstrip patch antenna array design is presented. This antenna is designed at 5.8GHz on FR4 substrate with dielectric constant at 4.7 and 0.0025 tangent loss. The simulation start with single patch antenna and followed by the 2x1 antenna array using T-junction power divider. Different spacing between patches will be simulated in order to investigate the antenna performance in term of gain and sidelobes. This project was succesfully displayed the grating lobes start to appear at certain spacing distance. The overall of the project concludes that during simulation design, the spacing distance of d=λ/2 was the best spacing distance. However, during the measurement procedure, the S_{11}(dB) of d=λ/2 not exceed the -10dB requirement.**

Keywords—Patch antenna; rectangular array patch; gratin lobes; T-junciton power divider.

I. INTRODUCTION

The microstrip antenna is the rapid growing scope in the telecommunication industry[1]. Microstrip antennas are low profile, inexpensive to manufacture using modern printed-circuit technology, simple and conformable to planar or non-planar surfaces. However, the single patch microstrip antenna has disadvantaged which is low gain [2].

Common method to increase an antenna gain is by increasing the number of patches. Another preferable method to increase the antenna gain is by increasing the spacing distances between the patches [3]. There is a limitation in using the spacing variation technique. If the space exceed certain points, unwanted signal so called grating lobe will be produced.

This paper present the simulation result that design by using Computer Simulation Technology (CST) software. The simulation starts with a single Microstrip Patch Antenna(MPA) design based from fundamental antenna sructure calculation. After some modification made in single patch, this project continues with the 2x1 array patches antenna.The spacing distance starts with d= λ/2,then 3/4λ, λ and 3/2λ. Based on the simulation design scalar, the array patch had be fabricated. Then its been measured to collect the data.

II. METHODOLOGY

The design of this project can be classified into hardware design and hardware measurement implementation. The overall system work flow is briefly described in this section. Figure 1 shows the flow chart of the project.

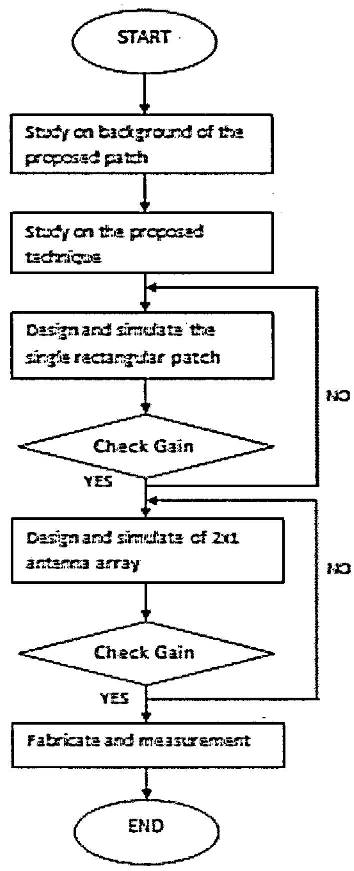

Figure 1: Flowchart of the project

This project start with study on background of the proposed patch. The rectangular patch antenna with inset-feed then being design as the proposed patch. Then, this project was continue with the study of spacing distance technique. Its the common method to increase an antenna gain by using spacing variation technique. After that, this study continue with the design and simulate of the single rectangular patch. Their patch performance need to be check in term of gain and return loss. Its simulation requirement for return loss was about lower than -10dB. This single patch can be proceed when the return loss meets the requirement. Later, a 2x1 antenna array been design and simulate based on the single patch. This array antenna used the transform and mirror technique to duplicate the patch. Their gain and return loss need to check once more whether its meet the requirement. Lastly, the fabrication process been done based on the simulation design scale. The measurement was performed by using the Vector Network Analyzer (VNA) apparatus. All the simulation and measurement result had been collected to analyse the return loss,gain and side lobes level.

III. BASIC ANTENNA STRUCTURE

The three most important parameters in designing rectangular patch antenna are width(W), length(L) and inset-feed(Y_0) as shown in Figure 2.

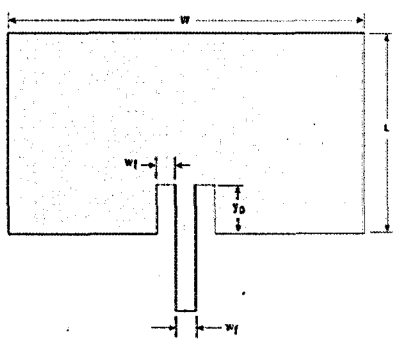

Figure 2: Topology of basic parameters for a microstrip-line inset-fed patch antenna, width (W), length (L) and distance of feed line from the edge (Y_0).

The equations to calculate the basic parameters of single rectangular patch antenna are given as:

i) The length of the patch,L

$$L = \frac{1}{2\sqrt{\varepsilon_{reff}}\sqrt{\varepsilon_o\mu_o}} - 2\Delta L \qquad (1)$$

ii) The width of the patch, W;

$$W = \frac{1}{2f_r\sqrt{\varepsilon_o\mu_o}}\sqrt{2/(\varepsilon_r + 1)} \qquad (2)$$

iii) The inset-feed of the antenna, Y_0;

$$Y_0=10^{-4}[0.001699er^7+0.13761er^6-6.1783er^5 +93.187er^4-682.69er^3+2561.9er^2 -4043er+6697] \qquad (3)$$

IV. RESULT AND DISCUSSION

A. Simulation of single patch antenna design

Based on the equation given in part II, all the parameters of the patch are calculated as shown in Table 1.

Table 1: Calculated parameters of single patch antenna

Parameter	W	L	Y_0	Feed	Substrate
Value	16.4	12.3	3.2	3.2	w=25.96 y=21.92

Figure 3 shows the graph of before and after optimization. Before optimization, the minimum value of S_{11}(dB) was at 5.325GHz and after optimization have been made, the S_{11}(dB) obtained was at the desired resonant frequency which is 5.8GHz. Details result comparison before and after optimization for single patch antenna is presented in Table 2.

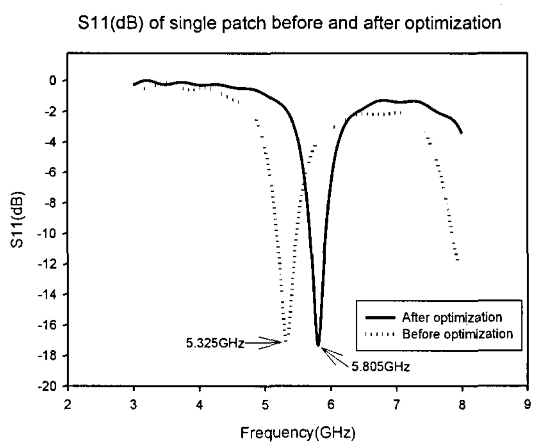

Figure 3: Response of single patch before optimization and after optimization

Table 2: Comparison before and after optimization for single patch antenna

Before Optimization		After Optimization	
S_{11}(dB)	f_0(GHz)	S_{11}(dB)	f_0(GHz)
17.198	5.325	17.345	5.805

B. Simulation of 2x1 antenna array design

The power divider is one of the most frequently used components in RF and microwave systems for power division and/or combination ratio as N-port network. Wilkinson power divider and T-junction power divider are the two conventional types of power dividers that have been used in the array antenna design [4].

Power divider used in this paper is T-junction type as shown in Figure 4. The T-junction is the earliest transmission line power dividers. This power divider is a fundamental passive component in micro-wave and millimeter-wave monolithic circuits. The characterization of its transmission and reflection properties is a topic of regularly interest [7].

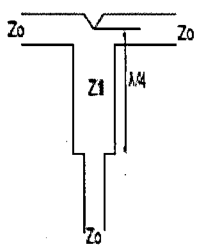

Figure 4 : T-junction power divider

Each port of antenna patch has 50Ω (Z_0) line input impedances and a quarter-wave matching transformer with an impedance of 35.38Ω (Z_1) [4].
The design of 2x1 antenna array patches with the T-junction power divider was displayed in the Figure 5 below. The patches was designed with spacing distance of d= λ/2 [5].

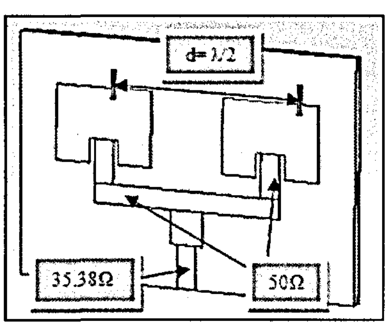

Figure 5: A 2x1 array antenna with T-junction power divider

The wavelength at designed frequency of 5.8GHz was calculated in order to determine the spacing distance between two patches. The calculated wavelength is shown below;

$$wavelength,\ \lambda = \frac{c}{f} = 51.72mm$$

$$\lambda/2 = 25.86mm$$

$$3/4\lambda = 38.79mm$$

$$3/2\lambda = 77.58mm$$

Figure 6 shown the result of MPA with spacing, d= λ/2 based on the value calculated above. The minimum S_{11}(dB) is -12.645dB at 5.8GHz.

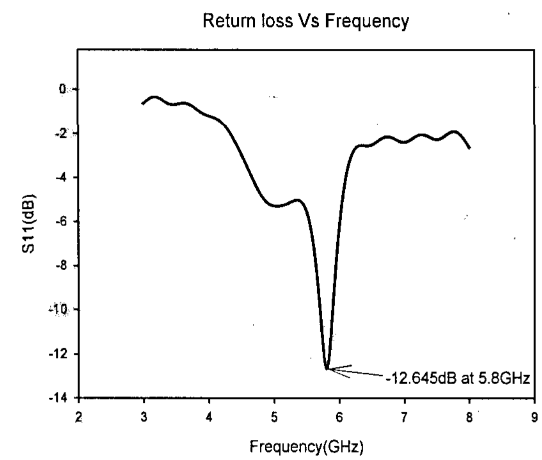

Figure 6: Graph of S_{11}(dB) against frequency power divider at spacing distance of λ/2

Figure 7 shows the simulation result of the impedance of the inset-feed port. Line impedance shows the matched port of 49.97Ω.

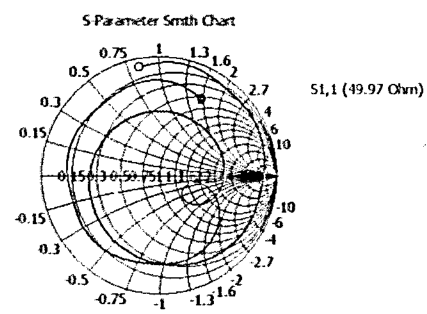

Figure 7: Smith Chart of the S-Parameter

In this study, the grating lobe starts to present as its power divider spacing distance are increased. In fact, the amplitude of grating lobes is significantly affected by patch size, the number of an array elements, frequency, and bandwidth [5]. The simulation been made based on the calculation above. Detail simulation result is presented in the Table 3.

Table 3: Result simulation from diffrent spacing

Spacing distance(d)	Directive gain(dB)	S_{11}(dBi)	Side Lobe(dB)
λ/2	7.665	- 14.001	-9.942
3/4λ	7.788	- 16.951	-0.947
λ	8.891	- 17.690	2.051
3/2λ	9.741	- 19.079	4.699

Based on the simulation result shown in Table 3, spacing of d=λ/2 has the lowest side lobe level which is -9.942dB and the directive gain is the smallest value that is 7.665dB. Meanwhile, d=3/2λ has the highest directive gain that is 9.741dBi but also have highest side lobe level that is 4.699dB.The simulation results shown in Figure 7.

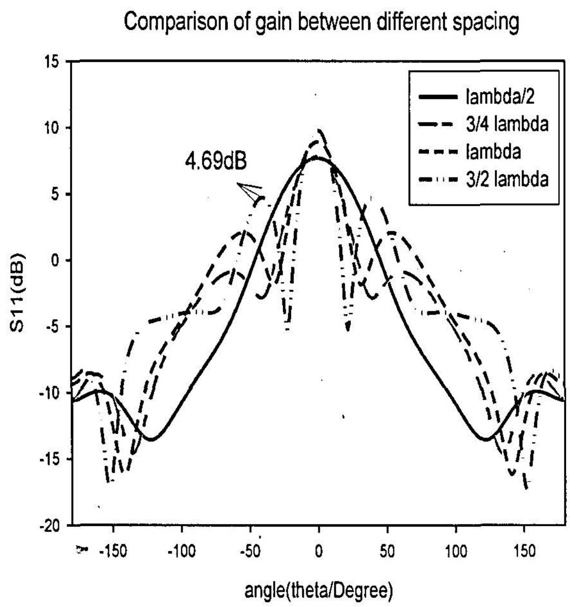

Figure 7: Graph comparison of gain between different spacing

C. Measurement Result Double Patch With d=λ/2 and d=3/2λ

The measurement was performed by using a Vector Network Analyzer (VNA). Figure 8(a) and 8(b) shows both fabricated circuits.

(a)

(b)

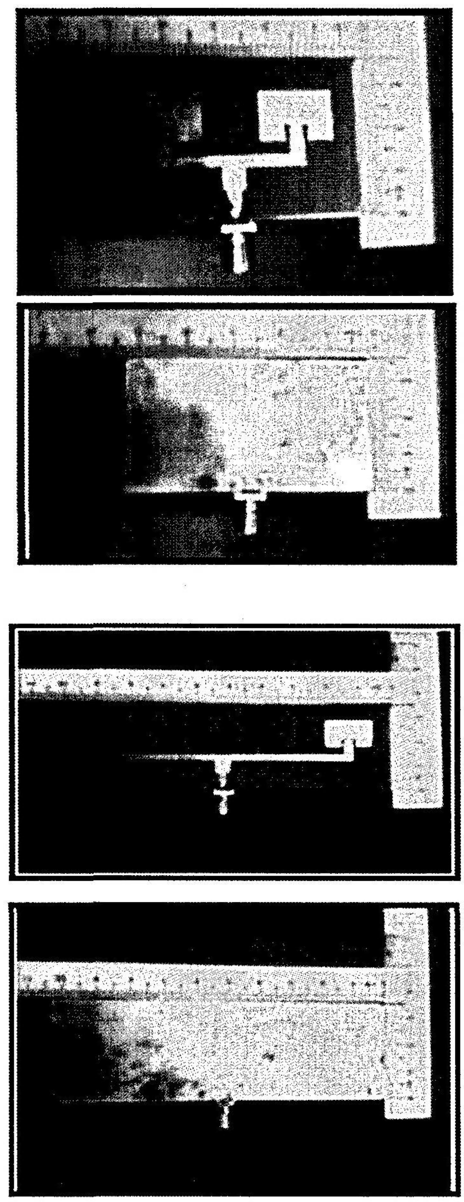

Figure 8 (a) Double patch with d=λ/2 and
(b) Double patch with d=3/2λ.

Figure 9(a) show the graph measurement result for double patch d=λ/2 MPA and figure 9(b) show the graph measurement for double patch d=3/2λ MPA.

(a)

(b)

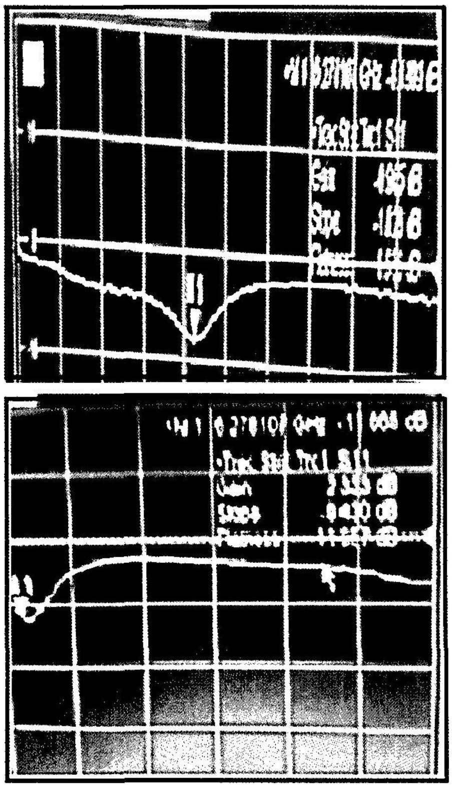

Figure 9(a) Double patch with d=λ/2 and
Figure 9(b) Double patch with d=3/2λ , show the output result S_{11} (dBi) against frequency (GHz).

Based on the graph measurement shown in Figure9(a) and Figure9(b), details result of this two spacing distances are shown in Table 4.

Table 4 : Comparison between double patch with d=λ/2 and double patch with d=3/2λ

D= λ/2		D=3/2λ	
S_{11}(dB)	f_0(GHz)	S_{11}(dB)	f_0(GHz)
-8.21	6.27	-11.67	6.27

V. CONCLUSION

In this paper, simulation data was demonstrated the concept of two array antenna element that having different spacing. The comparison of the return loss(S_{11} in dBi) and gain(dB) of the proposed antenna was done.Using varified spacing distance between the two array element, it produce better gain-to-side lobe ratio. Another method need to be use for the research purposes to reduce the grating lobes. A new metametarial patch antenna is suitable to reduce the grating lobes besides enhance the antenna gain [6].

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VII. REFERENCES

[1] Fan Yang and Yahya Rahmat-Ramli, "Electronic Band Gap structures in antenna" Electromagnetic Band Gap Structure in Antenna Engineering, Cambridge University Press, 2009

[2] Constantine A. Balanis, "Microstrip Antennas" *Antenna Theory Third Edition Analysis and Design*, John Wiley & Sons, Inc Publication, Copyright 2005

[3] Ramesh Gharg, Prakash Bhartia,"Microstrip Antenna" Microstrip Antenna design Handbook, Artech House, Copyright 2000

[4] A.Mohd Tarmizi, M.T. Mohd Nor, and R.Abdolee, "Reconfigurable Microstrip Patch Antenna Array With Beam Shaping", Wireless Communication Researsh Laboratory (WCC), University Teknologi Malaysia,Johor,Malaysia.

[5] JR James & P S.Hall, "Handbook of Microstrip Antennas, Volume 2, Peter Peregrinus Ltd, Copyright 1989.

[6] Saenz E,A.Ederra,Student Member IEEE, and de Maagt, Senior Member IEEE, "A Metamaterial T-Junction Power Divider, IEEE explore

[7] M.N.Md.Tan[1], T.A.Rahman[2],S.K.A.Rahim[2], and M.T.Ali[1], S.Subahir[1], "Backlobe Reduction Using Mushroom-Like EBG Structure", Faculty of Electrical Engineering, University Teknologi Mara (UiTM) Shah Alam, Malaysia.