Voltage Controlled Ring Oscillator for RF Applications in 0.18µm CMOS Technology

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ABSTRACT
A compact and power efficient high performance Voltage Controlled Oscillator (VCO) is a must in analog and digital circuits especially in the communication system. But the best trade-off among the performance parameters is a challenge for researchers. In this paper, a design of a compact 3-stage differential voltage controlled ring oscillator (VCRO) with low phase noise, low power and higher tuning bandwidth is proposed in 0.18µm CMOS technology. The VCRO is designed with symmetric load and positive feedback techniques to achieve higher gain and minimum delay. The proposed VCRO can operate at tuning range of 3.9-5.0 GHz at 1.6V supply voltage. The circuit consumes only 1.0757 mW of power and produces -129dbc/Hz. The total active area of the proposed VCRO is only (11.74 x 37.73) µm2. Such a VCO can be the best choice for compact and low-power RF applications.

Key Words: CMOS, VCO, VCRO, Oscillator.

INTRODUCTION
Voltage controlled oscillator with low power, low phase noise and wide range of tuning frequency is widely used in various applications especially in the field of wireless communication system. A variety of technologies such as BiCMOS, SiGe, CMOS, InP, GaAs etc. has been used to fabricate VCOs. Among the all, CMOS has been dominated nearly three decades because of its rapid advancements and continual downscaling (Jalil et al., 2013; Kader et al., 2012; Sallah et Al., 2012). This enabled the researchers to design low-cost small-size VCOs with higher frequency, lower power and lower phase noise parameters for different applications such as RFID, WLAN, Zigbee, Bluetooth etc. (Uddin et al., 2013; Yasin et al., 2006; Khaw et al., 2004; Rahman et al., 2010). However, designing a low power and a low phase noise VCO is still a challenge faced by the semiconductor industries due to trade-offs among the core performance parameters such as phase noise, power consumption, circuit speed, chip area, tuning frequency, stability etc. (Jalil et al., 2012; Saini, 2013).

There are mainly two types of VCOs utilized in different applications; inductance-capacitance (LC-tank) oscillators that generates harmonics oscillation and ring oscillators for relaxation oscillation wave. LC oscillators are typically used in wireless transceivers due to their higher linearity and good phase noise performance (Ghonondi and Naimi, 2011). However, this type of VCO exhibits relatively narrow tuning range, which further decreases with the supply voltage (Arakali et al., 2009). The main disadvantage of the designs is it requires a large chip area and suffers from substrate losses because of high conductivity of the substrate regardless of scaling (Tanabe et al., 2011). Therefore, to overcome the design limitations of LC oscillators in CMOS, ring type VCOs are introduced.
In contrast, ring type VCO (VCRO) offers a wider tuning range, lower power, smaller size and lower cost design (Jalil et al., 2012). Moreover, VCRO is easy to integrate with other circuits which makes it appropriate for many applications. A typical ring oscillator consists of a number of inverting amplifiers or delay stages coupled in a positive feedback loop as shown in Fig. 1. In order to achieve an oscillation, the circuit must provide a phase shift of 2π and have a unity voltage gain at the oscillation frequency (Docking and Sachdev, 2003). Differential configuration of VCRO is preferred to single ended topology for better stability at high frequencies, common-mode rejection of supply and substrate noise performance (Toh and McNeill, 2003).

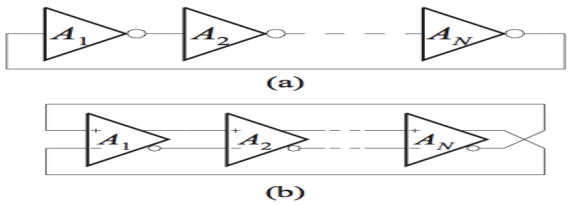

Fig. 1. Differential Delay Stage Configuration.

A differential VCRO which made of a number N of delay cells will oscillate at a frequency (fosc) given by,

$$f_o = \frac{I_{ss}}{2NV_{sw}C_L} \qquad (1)$$

where the CL is the total equivalent capacitance of the load, VSW is the maximum single ended voltage swing at the output of each delay cell.
The total power consumption for a differential ring oscillator can be represented as

$$P = NV_{DD}I \qquad (2)$$

where VDD is the supply voltage of the VCRO.

In this paper, a design of a compact 3-stage differential voltage controlled ring oscillator (VCRO) with low phase noise, low power and higher tuning bandwidth is proposed in 0.18µm CMOS technology. The VCRO is designed with symmetric load and positive feedback techniques to achieve higher gain and minimum delay. Such a VCRO will be very useful for RF transceivers for various applications.

METHODOLOGY

The proposed VCRO is designed in 0.18 µm CMOS technology by using Mentor Graphics IC Design environment. The differential configuration is chosen so that the oscillation frequency could be increased and at the same time reduce the power consumption. By minimizing the number of stages, the circuit's power consumption can be reduced significantly. The challenging part in designing a VCRO circuit is to design a circuit that can achieve the best parameter of oscillation frequency, power consumption and noise phase performances without compromise the quality of the VCO.

The basic structure of delay cell used in this study is based on the delay cell designed by (Kim et el., 2013). The VCRO utilizes 4 stages of delay cells and operates from 485.7 to 1011.6 MHz with very small power consumption of 10 mW. The reference delay cell is shown in Fig. 2. In this work, the load circuit of the delay cell is modified to use a symmetric load configuration. This helped to reduce the number of transistors used in the schematic circuit. The delay cell with symmetric load can improved the linearity of the load thus improves the power supply rejection ratio. Both transistors in the symmetric configuration will swing from the linear region to the saturation mode based on the control voltage (Tuan et al., 2008).

Cao et el. (2009) suggested positive partial feedback technique to provide the necessary bias condition for the oscillation of the circuit (Tuan et al., 2008). This technique helps to increase the effective transconductance of the circuit which in turn results increased gain but maintains the same total power levels compared to a conventional delay cell. The delay cell, with positive partial feedback consisting of transistors MN3 and MN4, is shown in Fig. 3.

Thabet et el. (2011) used the same feedback method in their VCRO circuit. The positive feedback was added to the full differential CMOS amplifier in order to reduce the delay period so that the overall speed of circuit operation can be improved (Thabet et el. 2011). The delay cell with positive feedback circuit is shown in Fig. 4.

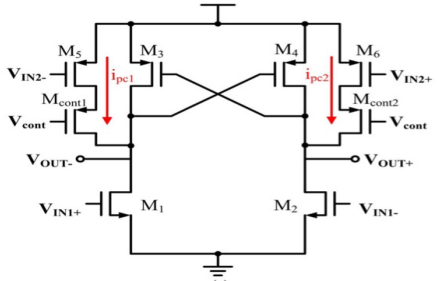

Fig. 2. Basic Structure of a Delay Cell (Kim et al., 2013).

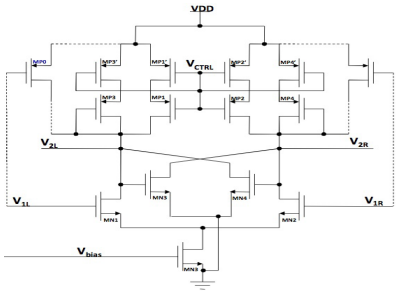

Fig. 3. Delay Cell with Partial Feedback (Tuan et al., 2008).

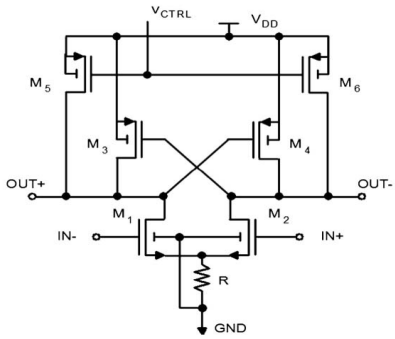

Fig. 4. Delay Cell Design with Positive Feedback (Thabet et el. 2011).

Based on the research made earlier, a modified positive feedback element is introduced in the basic circuit to increase the circuit gain and overall circuit speed. The proposed delay cell will consist of four pMOS and four nMOS transistors. Each delay cell will have 2 outputs; Output1 and Output2, which located at the end of positive feedback circuit. There will be 2 inputs to drive the symmetric load circuit, which are 1L and 1R. Another 2 inputs, 2L and 2R will be on the bias circuit. The proposed delay cell and the differential configuration of the delay cell are shown in Fig. 5 and Fig. 6 respectively. The stick diagram for the proposed delay cell is shown in Fig. 7.

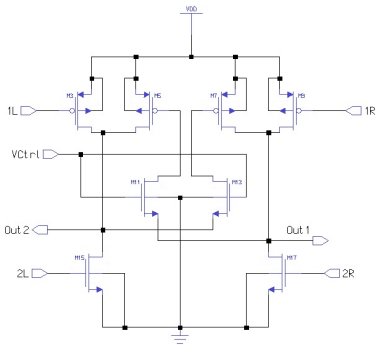

Fig. 5. Proposed Delay Cell Structure.

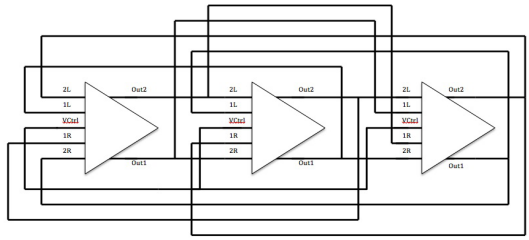

Fig. 6. Proposed 3 Delay Cell Configuration.

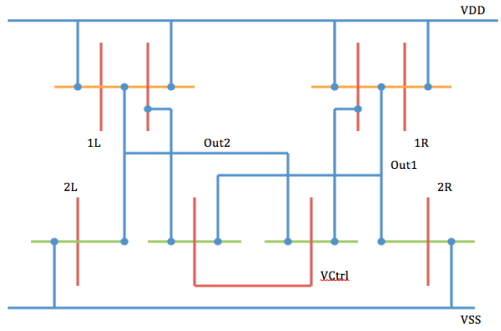

Fig. 7. Proposed Delay Cell Structure.

RESULTS AND DISCUSSION

The proposed VCRO for RF applications is designed and simulated in 0.18-µm CMOS process. Design Architect (DA-IC) and IC station tools of Mentor graphics are used to measure the performance of the oscillator. In this study tuning range, phase noise and power dissipation of the oscillator at different supply voltage and control voltage are evaluated.

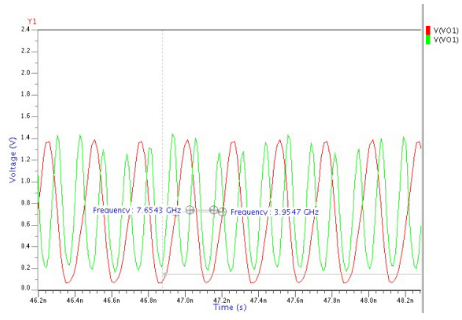

Fig. 8. Different Output for VDD of 1.6V and 2.3V.

The output waveform of the proposed VCO for supply voltage (VDD) 1.6 v and 2.3 v is illustrated in Fig. 8. From this figure it is evident that the proposed VCRO produce better waveform for 1.6V supply compared to 2.3V supply although the frequency of oscillation are different. For 1.6V supply, the VCRO produces

3.95GHz while for 2.3V it produces 7.65GHz frequency signal. Even though the frequency is lower, the output at low supply voltage is better in shape but it experiences slight jitter in the waveform. The operating temperature of the circuit was set to 27oC.

Table 1 Frequency and Power Consumption with Different VDD

V_{DD} (V)	V_{Ctrl} (V)	Frequency (GHz)	Power Consumption (mW)
1.6	1.6	3.955	1.0757
1.6	1.8	4.424	1.0757
1.6	2.0	5.076	1.0757
1.8	1.8	4.487	1.575
2.0	1.8	5.340	2.1806
2.0	2.0	5.361	2.1806
2.2	1.6	7.268	2.959
2.2	1.8	6.318	2.959
2.2	2.0	4.912	2.959
2.3	1.6	7.654	3.3639

In order to validate the oscillator for wide frequency range as well as to analyze the effect of different voltages on frequency and power consumption of the circuit, it is simulated with different values of VDD and VCtrl. The complete result is accumulated in Table I. From Table 1, it is clear that the higher the VDD, the higher is the power consumed by the VCRO. On the other hand, the power dissipation is independent of VCtrl. The frequency of oscillation can be increased with the increased value of VCtrl but the power dissipation of the circuit remains the same. The optimum range frequency for lowest power consumption is between 3.9 – 5.0 GHz at 1.6V power supply. The performance parameters of the VCO are summarized in the Table II.

Table 2 Summary of the Parameters of Proposed VCRO

Parameters	Value
Technology	0.18 um CMOS
Delay Stage	3
Operation Mode	Differential
Supply Voltage	1.6
Power Consumption	1.0757 mW
Tuning Range	3.9 – 5.0 GHz
Phase Noise (dBc/Hz)	-129
Area	11.74 x 37.73 um^2

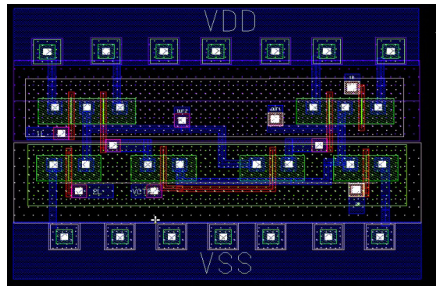

Fig. 9. Layout of a Single Delay Cell.

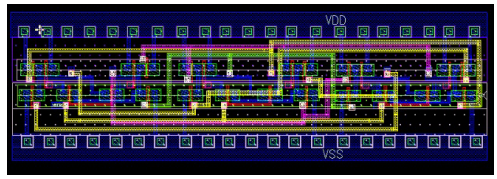

Fig. 10. Layout of Three Stage Delay Cell.

The performance comparison of this VCO with previously reported VCOs are given in Table III. The proposed VCRO exhibits almost 90% less power consumption compared to the reference circuit (Kim et al., 2013). The phase noise is lower and the tuning range is also found bigger compared to reference. The total chip area of this VCO is the smallest. All these desired parameters are compensated with higher supply voltage of 1.6 V. The layout of a single delay cell and the complete layout of the VCO are shown in Fig. 9 and Fig. 10, respectively. Total area of the proposed 3-delay cell is only 11.74 x 37.73 µm2 which is the smallest. Such a VCO can be the best choice for compact and low-power RF applications.
Table 3 Performance Comparison of Voltage Control Ring Oscillator

Mode	(Kim et al., 2013)	(Tuan et al., 2008)	(Thabet et el. 2011)	(Raman and Sarin, 2013)	(Jalil et al., 2013)	This work
Technology (µm)	0.065	0.065	0.35	0.18	0.18	0.18
Number of delay stages	4	2	3	3	3	3
Supply Voltage (V)	1.0	0.6	3.3	1.8	1.8	1.6
Tuning range (GHz)	0.48-1.01	0.3-0.9	0.4-1.1	1.3 – 5.7	2.36-2.85	3.9-5.0
Power (mW)	10	0.212	7.48	0.51	6.99	1.07
Phase noise (dBc/Hz)	-110	-132	-126	-	-112	-129
Area (mm²)	0.022	-	0.235	-	0.003	0.00004

CONCLUSION

A modified 3-stage differential voltage controlled ring oscillator with low power, low phase noise and higher tuning frequency range has been proposed using 0.18um CMOS technology. A symmetric load with low phase noise characteristic is applied on the proposed VCRO. A positive feedback is implemented on the circuit to minimize the delay time thus speed up the overall circuit operation's timing. The result indicates the VCRO be able to operate at tuning range of 3.9-5.0 GHz at 1.6V supply voltage. The circuit consumes 1.0757 mW of power and produces -129dbc/Hz of phase noise. The total active area of the proposed VCRO is 11.74 x 37.73 µm2. The proposed VCRO is able to operate at wider frequency range and at low supply voltage at lower power consumption.

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