UNIVERSITI TEKNOLOGI MARA

CHARACTERIZATION OF DEFECTS GENERATED BY COPPER ELECTROCHEMICAL PLATING PROCESS ON SILICON WAFERS

YASMIN BINTI ABDUL WAHAB

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Faculty of Electrical Engineering

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Candidate's Declaration

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Candidate's Name: YASMIN BINTI ABDUL WAHAB

Candidate's Signature: .....

Date: 4th July 2008

ABSTRACT

With the rapid adoption of dual-damascene copper (CuDD) processing as semiconductor device features shrink into deep-submicron process, the copper electrochemical plating (ECP) is emerging as one choice for Cu metallization in multilevel interconnects. Copper processing has brought about an increased need to understand and predict desirable properties of the physical vapor deposition barrier and seed deposition, electroplating, chemical-mechanical polishing (CMP) as well as any thermal treatments that required stabilizing and annealing copper. Instead, defectivity is gaining momentum in Cu integration due to new Cu interconnects schemes and increasingly stringent process control requirements post some serious challenges in modern microelectronics devices. As a result, defectivity has driven a significant rise in process failure rates and has had a strong impact on the back-end-of-line (BEOL) processes.

This project investigated the characterization of defects generated by copper electroplating process on He In-Situ and furnace annealed electro-plated copper films on p-type bare silicon wafers. A post ECP He In-Situ anneal processing was carried out over a 60 ºC to 180 ºC temperature range, with anneal duration times ranging from 6 seconds to 2 hours and the wafers began to be ramped at over 100 ºC with less than a minute soak time. For the furnace anneal, the wafers were loaded for almost an hour with less than 200 ºC soak temperature. Specifically, impacts originated from the defects such as influences on yield lost are being investigated.

This study improved a novel procedure of defect measurement, defect source analysis and static code analysis that was employed to identify the different types of defects generated progressively by post copper barrier seed, electrochemical plating, anneals and chemical mechanical planarization. To characterize the modes of action of defects in such processes, we employed constructive and analytical methods to analyze the interaction between defects from incoming and electroplating process and analyzing with scanning electron microscope (SEM) and covers process parameters perspective. Based on the design of experiments data, a new defect characterization scheme that takes defect generation mechanism and potential source into account has been proposed. The proposed scheme improves to differentiate between plating and CMP induced defects and flaws that were generally categorized as missing copper could have resulted from corrosion or scratches during polishing process from incomplete filling of fine features after plating. The study indicates the potential of right inspection and analysis approach of defects characterization can improve entire process modules and indirectly make CuDD technology production-worthy.

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CHAPTER 1

INTRODUCTION

1.1 Copper Electro Plating in Semiconductor Fabrication

Multilevel copper interconnection has been extensively used in the era of ultra large-scale integrated (ULSI) circuits, and copper electroplating is widely accepted today as a preferred method of depositing copper due to its superfilling capability. Owing to its lower bulk electrical resistivity (1.7 μΩ cm) and higher electromigration resistance, Cu has begun to replace Al as the choice of interconnecting material [1]. Nonetheless, Cu is a fast-migrating impurity in silicon-based devices, and its inherent chemical reactivity renders it susceptible to corrosion and oxidation. Hence, the key to integrating Cu interconnecting technology is suitable encapsulant that acts both as an effective barrier to Cu diffusion and an adhesion promoter to the adjoining dielectric and metal films while maintaining the overall metal interconnection performance.

Copper (Cu) electroplating using special chemistries and processes to fill the fine submicrometer trenches and vias of damascene architectures without voiding is a key process in the fabrication of Cu interconnects. Electroplating is being used in an ever-increasing number and in new types of applications of engineering. The ability to predesign the properties of surfaces by deposition of thin multilayers via electroplating represents yet another new avenue to produce new materials and this directly brings advantages to semiconductor fabrication.

More specifically, "Electrochemical Plating" refers to the structures that need to be filled are trenches that compose vias. Trenches are typically micron sized and have