UNIVERSITI TEKNOLOGI MARA

LOGICAL EFFORT BASE ADDER CIRCUITS TRANSISTOR SIZING USING CONSTRICTION FACTOR AND MUTATIVE VARIANTS OF PARTICLE SWARM OPTIMIZATION ALGORITHM

MUHAMMAD AIMAN BIN JOHARI

Thesis submitted in fulfilment
of the requirements for the degree of
Master of Science

Faculty of Electrical Engineering

June 2015

AUTHOR'S DECLARATION

I declare that the work in the thesis was carried out in accordance with the regulations of Universiti Teknologi MARA. It is original and is the result of my own work, unless otherwise indicated or acknowledged as referenced work. This thesis has not been submitted to any other academic institution or non-academic institution for any degree of qualification.

I, hereby, acknowledge that I have been supplied with the Academic Rules and Regulations for Post Graduate, Universiti Teknologi MARA, regulating the conduct of my study and research.

Name of Student	:	Muhammad Aiman bin Johari
Student I.D. No.	:	2010229574
Programme	:	Master in Electrical Engineering (EE780)
Faculty	:	Faculty of Electrical Engineering
Thesis Title	:	Logical Effort Base Adder Circuits Transistor Sizing Using Contriction Factor And Mutative Variants Of Particle Swarm Optimization Algorithm
Signature of Student	:	
Date	:	June 2015

ABSTRACT

In Semiconductor world, the design and fabrication of Integrated Circuit (IC) associated with development time, operating speed and power requirements. The goodness of each design must be evaluated before it is chosen, especially on speed of the circuits where it represent the time taken to execute a specific function or most commonly known as delay. Conventional methods use repetitive manual testing guided by Logical Effort (LE). LE provides an easy way to compare and select circuit topologies, choose the best number of stages for path and estimate path delay. The proposal of Particle Swarm Optimization (PSO) with constriction factor (PSO-CF) and mutative variants (PSO-M) presented in this thesis attempts to create an automated process of transistor sizing optimization. The method attempts to get the target circuit delay on tested circuit's critical path based on LE calculation that accepts generated transistor size by both PSO variants as inputs to fitness function. The optimization of the transistor size will stop if maximum iteration reached of different between PSO's found delay and objective delay is very small (near or similar to '0'). Various parameters, such as swarm size and iterations were tested under different initial positions to verify PSO's performance on a adder circuits namely modified half-adder (M-HA), modified full-adder (M-FA) and modified ripple-carry adder (M-RCA). The experiments reported in this thesis showed that both PSO variants were efficient to automatically find the optimum transistor size with solution range of $[10^{-2}, 10^{-15}]$ for PSO-CF and $[10^{0}, 10^{-16}]$ for PSO-M.

TABLE OF CONTENTS

	Page
AUTHOR'S DECLARATION	ii
ABSTRACT	iii
ACKNOWLEDGMENTS	iv
TABLE OF CONTENTS	v
LIST OF TABLES	viii
LIST OF FIGURES	ix
LIST OF ABBREVIATIONS	xiii
CHAPTER ONE: INTRODUCTION	1
1.1 Research Background	1
1.2 Problem Statement	2
1.3 Proposed Method	2
1.4 Objectives of the Study	4
1.5 Scope of the Study	4
1.6 Outline of the Thesis	5
CHAPTER TWO: LITERATURE REVIEW	6
2.1 Introduction	6
2.2 Arithmetic Logic Unit (ALU)	6
2.3 Types of Adder Circuits	9
2.3.1 Modified Half Adder circuit (M-HA)	9
2.3.2 Modified Full Adder circuit (M-FA)	11
2.3.3 Modified Ripple Carry Adder Circuit (RCA)	12
2.4 Delay in Integrated Circuits	13
2.5 Logic circuit design	16
2.6 Introduction of Logical Effort (LE)	18
2.7 Introduction of Particle Swarm Optimization (PSO)	19
2.7.1 Constriction Factor Variant	20
2.7.2 Mutative Factor Variant	21
2.8 Chapter Conclusion	22

CHAPTER THREE: THEORETICAL BACKGROUND 24
3.1 Introduction 24
3.2 Logical Effort (LE) 24
3.2.1 LE for Single-stage Circuit 24
3.2.2 LE for Multi-stage Circuits (Without Branching) 26
3.2.3 LE for Multi-stage Circuits (With Branching) 27
3.2.3.1 M-HA Delay Calculation (Path_1) 29
3.2.3.2 M-HA Delay Calculation (Path_2) 31
3.2.3.3 M-HA Delay Calculation (Path_3) 32
3.2.4 Least Delay using LE 34
3.2.5 Transistor Sizing using LE 35
3.3 Particle Swarm Optimization Algorithm (PSO) 37
3.3.1 PSO with Constriction Factor Variant (PSO-CF) 38
3.3.2 PSO with Mutative Factor Variant (PSO-M) 39
3.3.3 PSO Parameters 40
3.4 Transistor Sizing using PSO Guided by LE 41

CHAPTER FOUR: METHODOLOGY 42
4.1 Introduction 42
4.2 Hardware Description 42
4.3 Description of Experiment 42
4.3.1 Delay and Transistor Size Calculation 43
4.3.2 Design and Implementation of PSO algorithm 44
4.3.3 Validation of PSO algorithm 44
4.3.3.1 Parameter Used to Optimize RF 46
4.3.4 Implementation of Adder's Fitness Function 47
4.3.5 Perform Optimization & Analyze Solution 49
4.4 Chapter Conclusion 50

CHAPTER FIVE: RESULTS 52
5.1 Introduction 52
5.2 Delay and Transistor Sizing using LE 52
5.2.1 M-HA Delay and Transistor Size Calculation 52