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Foreword

It is indeed a proud moment for the University Publication Centre (UPENA) of UiTM Pulau Pinang for having realised the publication of the sixth volume of the Esteem Academic Journal UiTM Pulau Pinang. In fact, it is the undivided support and all-round commitment from all those who were directly and indirectly involved in this project that was the pivotal factor for this success.

On behalf of UPENA UiTMPP, I would like to, first and foremost, express my sincerest gratitude to Associate Professor Mohd Zaki Abdullah, Director of UiTM Pulau Pinang, Associate Professor Dr Mohamad Abdullah Hemdi, Deputy Director of Academic Affairs and Associate Professor Ir. Damanhuri Jamalludin, Deputy Director of Research, Industry Linkages, Development & Maintenance for their unwavering support and being such a driving force towards this successful endeavour.

Not to be forgotten also is the service rendered by the distinguished panel of external reviewers for their constructive comments and criticisms in ensuring that the papers published in this issue would be of the highest quality. Similarly, the panel of language editors who had worked tirelessly towards ensuring that the papers published were linguistically perfect. To both these groups, UPENA is in awe of your efforts and salutes you!

UPENA is also impressed with the nature of papers submitted for publication. While this issue comprises all engineering based articles, it covers a wide array of sub-engineering disciplines. Kudos to these writers! UPENA sincerely appreciates their efforts and hopes more of our staff will follow in their footsteps.

Finally, research and publication are integral parts of an academic's life at any institution. Apart from being an institutional requirement, it is also essential for our own continuous self-development and knowledge expansion. To this effect, UPENA hopes to play a significant role by providing the platform upon which our staff can realise their dream. So, it is our hope at UPENA UiTMPP that lecturers will take up the challenge and start to publish more vigorously from now on.

Rasaya Marimuthu
Chief Editor
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(Engineering)

Fabrication and Characterization of 0.24 Micron CMOS Device by Using Simulation

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ABSTRACT

Simulation and analyzing the electrical characteristics of 0.24 micron CMOS device was done by using Silvaco TCAD. Electrical characteristics were carried out by using Atlas device simulator, while for simulation the process was carried out by using Athena process simulator to modify theoretical values and obtain more accurate process parameters. The electrical parameter was extracted to investigate the device characteristics. Several design analyses were performed to investigate the effectiveness of the advanced method in order to prevent the varying of threshold voltage. The electrical characteristics produce the graph of drain current versus drain voltage, I_D-V_D and drain current versus gate voltage, I_D-V_G. From I_D-V_G can be obtained the threshold voltage, V_T in which V_T for NMOS transistor is lower than V_T for PMOS transistor which is 0.6695V and -0.9683 V respectively. The gate length L_G obtained from the simulation for NMOS and PMOS is the same which is 0.235 micron and it is nearest to the scale for this research work.

Keywords: *P-channel MOS (PMOS), N-channel MOS (NMOS), 0.24 micron, drain current (I_D), drain voltage (V_D), and gate voltage (V_G).*

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Introduction

The electronic industry is the largest industry in the world with global sales over one trillion dollars since 1998. In the early twenty-first century, the industry has grown at an even higher rate to surpass the steel industry (Sze & Kwok, 2007). Integrated circuit (IC) technology has not resulted from reverse engineering of a crashed alien spaceship, as some UFO fans claim. It has taken many thousands of scientists, engineers and technicians more than 50 years of innovative, creative and industrious work to make IC technology what it is today. IC chip technology has changed our lives dramatically. Since then IC chips have been developed in complexity and usefulness to the point that hundreds, if not thousands, can be found in average households in developed countries. IC chips are the backbone of the computer industry and have spurred related technologies such as software and internet (Hong Xiao, 2002).

Much of the progress in semiconductor integrated circuit technology can be attributed to the ability to shrink or scale the devices. Scaling down MOSFETs has a multitude of benefits (Streetman & Sanjay, 2006). Geometric scaling of MOSFET transistor dimensions has been the primary method used to increase transistor speed and simultaneously reduce the cost per function. State-of-the-art MOSFETs are now being fabricated with effective gate lengths of only a few tens of nanometers, pushing conventional Si-based technologies into the nanoelectronics regime (Olsen, Kwa, Driscoll,Chattopadhyay & O'Neill, 2004).

The scaling theory, based on a constant electric-field, requires supply voltage, threshold voltage, gate length, and gate oxide thickness to be scaled down by a scaling factor. The doping level in the channel must be scaled up by the same scale factor. The junction depth of source and drain also needs to be scaled down to suppress the short-channel effect (MOSFET scaling, 2009).

The MOSFET transistor has been scaled down by using the Constant Field Scaling rules because it is easier and is assumed to avoid the high field problems (Teoh & Razali, 2006).

When the need for a million transistors to be fabricated on a single chip arises, power consumption becomes the first limiting factor for VLSI. CMOS circuits have provided the most logical solution due to their complementary nature of the n- and p-channel transistors, which consume much less power. In addition, at submicron regions, the process complexity of nMOS has become comparable to that of CMOS due to the scaling

down of device dimensions. Lastly, the performance difference between nMOS and pMOS has reduced drastically due to velocity saturation, thus making CMOS technology become more attractive in VLSI circuit (Toh, Mohd Rais, Roy, Rahman & Bambang, 1998).

As a result of the changing nature of integrated circuit manufacture, the nature and role of TCAD design tools will involve new solutions. For future hardware generation hardware designs, it is anticipated that web based solutions will play an increasing role in achieving TCAD and virtual prototyping aims for future and emerging technologies. Web-based solutions are expected to primarily take the form of large, interactive databases and de-localized compute engines (Campian, Profirescu, Alina, Florin, Eugen & Claudiu, 2003).

Scope of Work

The objective of the project was to simulate the process of fabrication and analyze the electrical characteristic for 0.24 micron NMOS and PMOS devices. Before the fabrication of the 0.24 micron CMOS, each process steps, ATHENA and ATLAS simulator in the SILVACO TCAD tool simulation need to be understood.

Methodology

Figure 1 shows the fabrication process for this device while Table 1 summarizes the used implantation condition parameters used in NMOS and PMOS fabrication.

The 0.24 micron devices should be tested electrically by using Silvaco-Atlas simulation. It is used to measure the current versus voltage which is in the form of I_D-V_D and I_D-V_G graph. From $I_D V_D$ graph, the drain current I_D used in the NMOS and PMOS device at different voltage gate applied could be obtained.

Furthermore, the threshold voltage, V_T can be extracted from the $I_D V_G$ graph. This value will be compared with real fabricated transistor. The Figure 2 shows the $I_D V_G$ graph (Lecture 3 Transistors, Wires, & Parasitics, 2005).

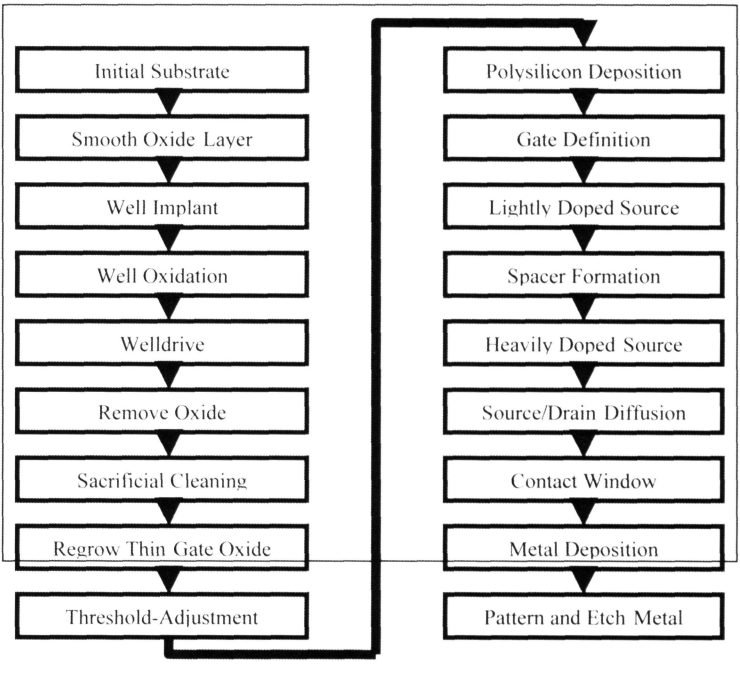


Figure 1: The Fabrication Process

Result and Discussion

Electrical Characterization

The analysis results are shown in the graph of drain current versus drain voltage, I_D-V_D and the drain current versus gate voltage, I_D-V_G. The characteristic curves of I_D-V_D of NMOS and PMOS was shown in Figure 3. From Figure 3, the circle line indicates higher V_{GS} and V_{DS} where short channel effect is more significant. This can be seen from the increase of I_D as V_D increases.

The transistor can function when the threshold voltage, V_T is in the range of $0.5881V < V_T < 0.7593$ for the NMOS and the PMOS is $-0.8314 < V_T < -1.0732$. The value of threshold voltage, V_T can be found from the I_D-V_G graph.

Table 1: The Parameters of NMOS and PMOS

Process	NMOS	PMOS
Silicon substrate	• 1×10^{15} cm^{-3} boron • <100> orientation	• 1×10^{15} cm^{-3} phosphorus • <100> orientation
Retrograde well	• 3×10^{13} cm^{-3} boron • 200 keV implant energy • 30 min, 1000 °C	• 6.8×10^{12} cm^{-3} phosphorus • 100 keV implant energy • 30 min, 1000 °C
Gate oxide	• 0.035 um gate oxide	• 0.035 um gate oxide
V_T adjust implant	• 9.5×10^{13} cm^{-3} boron • 45 keV implant energy	• 2.5×10^{13} cm^{-3} boron fluoride • 10 keV implant energy
Polygate deposit	• 200 nm polysilicon • 5 min, 900 °C	• 200 nm polysilicon • 5 min, 900 °C
LDD implant	• 1×10^{15} cm^{-3} arsenic • 30 keV implant energy	• 5.4×10^{14} cm^{-3} boron • 14 keV implant energy
Halo implant	• 3×10^{13} cm^{-3} boron • 30keV implant energy • 7° tilt	• 5.83×10^{12} cm^{-3} arsenic • 28 keV implant energy • 30° tilt
Spacer deposition	• 120 nm oxide	• 120 nm oxide
Source/Drain implant	• 5×10^{15} cm^{-3} arsenic • 60 keV implant energy	• 3×10^{15} cm^{-3} boron fluoride • 20 keV implant energy
Final Rapid Thermal Anneal (RTA)	• 1 min, 1000 °C	• 5 min, 900 °C

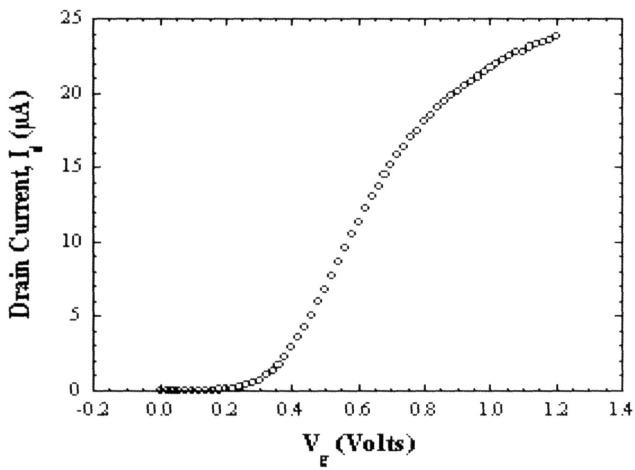
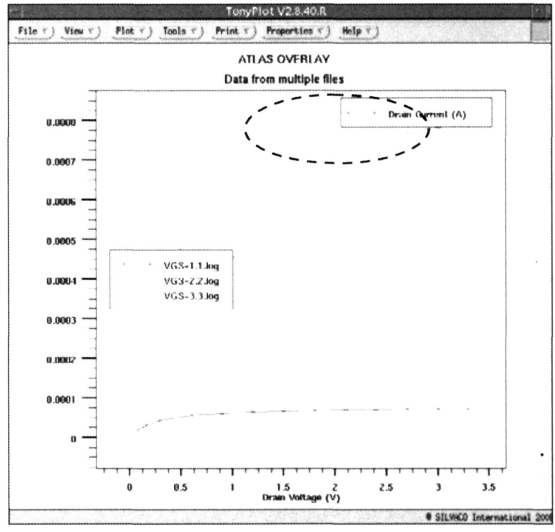
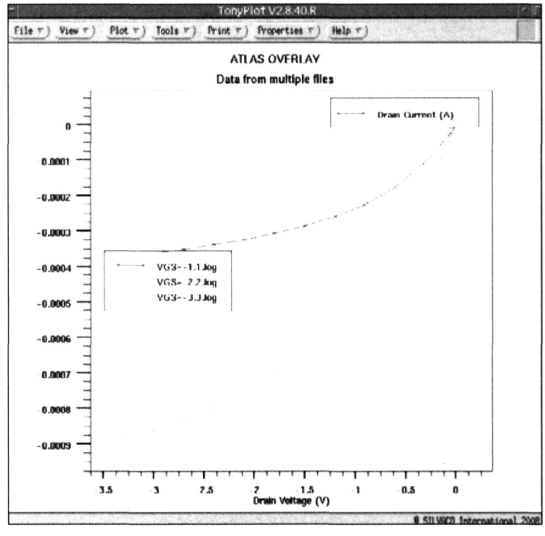


Figure 2: The I_D-V_G Graph for NMOS Transistor



(a)



(b)

Figure 3: The I_D-V_D curve for (a) NMOS and (b) PMOS

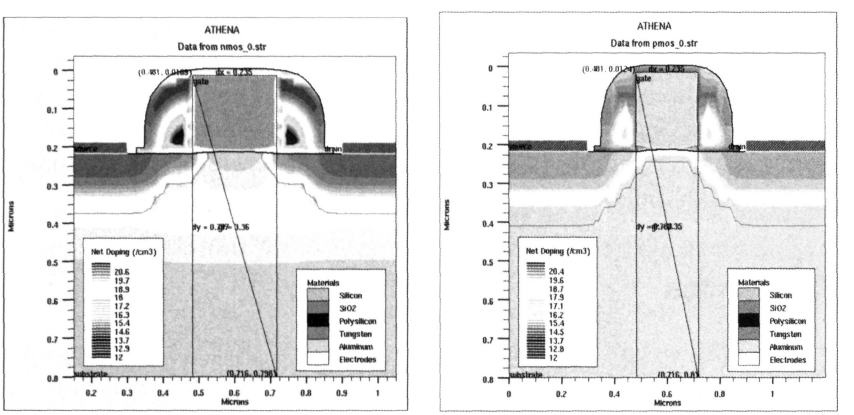
Table 2: The Comparison Threshold Voltages between Simulation and Wafer Sample

	Threshold Voltage, V_T (V)	
	NMOS	PMOS
Simulation	0.669503	-0.968358
Wafer Sample	0.4V	0.699V

From the Table 2, it is shown that the simulation result is in the range value of threshold voltage, V_T for NMOS and PMOS device, therefore the transistor is function as a normal transistor. From the wafer sample, the threshold voltage is not in the range, so the transistor does not function appropriately.

Material Characterization

Figure 4 shows the cross section of the final structure. Table 3 shows the material composition in the 0.24 micron NMOS and PMOS. It is shown that both devices exhibit 0.24 micron gate length after the simulation.



(a) (b)

Figure 4: The Final Device Structure for (a) NMOS and (b) PMOS

Table 3: The Materials Used for Component of Device of 0.24 micron NMOS and PMOS

Component of Devices	NMOS	PMOS
Substrate	Silicon (Si)	Silicon (Si)
Initial Substrate	Boron (B)	Phosphorus (P)
Retrograde Well	Boron (B)	Phosphorus (P)
Thick Oxide Layer	Silicon Oxide (SiO_2)	Silicon Oxide (SiO_2)
Halo Implant	Boron (B)	Phosphorus (P)
Gate Terminal	Polysilicon	Polysilicon
Source/Drain Contact	Tungsten	Tungsten
Source/Drain Extension	Arsenic (As)	Boron Fluoride (Bf_2)
Source/Drain Implant	Arsenic (As)	Boron Fluoride (Bf_2)

Conclusion

In conclusion, this project for the fabrication of 0.24 micron NMOS and PMOS is successfully fabricated by using Silvaco TCAD tool and analyzed. The analysis of the electrical characterization result shows that the NMOS transistor operation has higher mobility than PMOS transistor because the value of NMOS transistor is lower which is 0.6695V, than the value of PMOS transistor, which is -0.9683V. The short channel effect is more significant when at higher V_G and V_D. It can be seen from the increase of I_D as V_D increases. The simulation result was also compared to the real fabrication transistor or the wafer sample for the threshold voltage, V_T value. It shows that the simulation result has the value V_T in the accepted range. On the other hand, the result from the wafer sample is not in the range. Therefore, the simulated transistor can function as a normal transistor.

References

Ahmad, W.R.W., Kordesh, A.V., Ahmad, I., & Yew, P.T.B. (2006). *TCAD simulation of STI stress effect on active length for 130nm technology.* Semiconductor Electronics, 2006. ICSE'06. IEEE. 1038-1040.

Ben, G. Streetman & Sanjay Kumar Benerjee. (2006). *Solid State Electronic Devices*. Sixth Edition, Pearson Education.

Champian, I., Profirescu, O. –G., Ungureannu, A., Babarada, F., Lakatos, E., & Amza, C. (2003). *MOSFET simulation-TCAD tools/ packages*. Semiconductor Conference, 2003. CAS 2003. 2, 235-238.

Chang, S.K., Hag-Ju, C., Rino, C., Young-Hee, K. Chang, Y.K., Se J.R., Changhwan, C., & Jack, C.L. (2004). *The electrical and material characterization pf hafnium oxynitride gate dielectrics with TaN-gate electrode.* IEE Transaction on Electron Devices, 51(2), 220-227.

Chang, W. O., Kyoung, H. Y., & Min Sang. (2004). *Electrical characterization of partially insulated MOSFETs with buried insulators under source/drain regions.* Solid-state Device Research Conference, 2004. ESSDERC 2004. Proceeding of the 34th European. 233-236.

Chen, E., Heo, D., Hamai, M., Laskar, J., & Bien, D. (2000). *0.24 um CMOS technology for Bluetooth power applications.* Radio and Wireless Conference (RAWCON 2000) IEEE. 163-166.

Driussi, F., Esseni, D., Selmi, L., Buca, D., Malt, S., Luysberg, M., et al. (2007). *Fabrication, characterization and modeling of strained SOI MOSFETs with very large effective mobility.* Solid-state Device Research Conference, 2007. ESSDERC 2007. Proceeding of the 37th European. 315.318.

Fenouillet-Beranger, C. Faynot, O., Tabone, C., Colladant, T., Ferlet, V., Jahan, C., & Pelloie, J.L. (2001). *Characterization and simulation of STI isolation for 0.1um partially-depleted SOI devices.* SOI Conference, IEEE International. 87-88.

Ghibaudo, G., & Clerc, R. (2004). *Characterization and modeling issues in MOS structures with ultra thin oxides.* 24th International Conference on Microelectronics. 103-114.

Harrison, S., Munteanu, D., Autran, U., Cros, A. Cerruti, R., & Skotnicki, T. (2004). *Electrical characterization and modelling of high performance SON DG MOSFET.* Solid State Device Research

Conference, 2004. ESSDERC 2004. Proceeding of the 34th European. 373-37.

Hong Xiao. (2002). *Introduction of Semiconductor Manufacturing Technology*, Prentice Hall.

Lecture 3 Transistors, Wires, & Parasitics. (2008) [PowerPoint slides]. Retrieved from http://www.cpe.ku.ac.th/~pom/courses/204424/2005/Lecture03-2005.ppt.

MOSFET scaling. (2008). Retrieved from http://en.wikipedia.org/wiki/MOSFET

Olsen, S.H., Kwa, K.S.K., Driscoll, L.S., Chattopadhyay, S., & O'Neill, A.G. (2004). *Design, fabrication and characterization of strained Si/SiGe MOS transistors.* IEE Proceedings, Circuit, Devices System, 151(5), 431-437.

Ortolland, C., Orain, S., Rosa, J., Morin, P., Arnaud, F., Woo, M., & Stolk, P. (2004). *Electrical characterization and mechanical modeling of process induced strain in 65 nm CMOS technology.* Solid-state Device Research Conference, 2004. ESSDERC 2004. Proceeding of the 34th European. 137-140.

Quenette, V., Lemoigne, P., & Rideau, D. C. (2008). *Electrical characterization and compact modeling of MOSFET body effect.* ULIS 2008, 9th International Conference. 163-166.

Shang, H., Okorn-Schimdt, H., Ott, J., Kozlowski, P., Steen, S., Jones, E.C., & Hanesh, W. (2003). *Electrical characterization of Germanium p-channel MOSFETs.* IEEE Electron Device Letters, 24, 242-244.

S.M. Sze, & Kwok, K. Ng. (2007). *Physics of Semiconductor Devices*, Third Edition, A John Wiley & Sons, Inc., Publication.

Teoh Cheng Hong & Razali Ismail. (2006). *Device design consideration for nanoscale MOSFET using semiconductor TCAD tools.* IEEE International Conference, ICSE '06 Proceeding. 906-910.

Toh Hong Ting, Mohd Rais Ahmad, Roy Kooh Jinn Chye, Rahman Wagiran & Bambang Sunaryo Suparjo. (1998). *Device design, fabrication and characterization of 0.8 um CMOS technology*. ICSE '98 Proceeding. 147-151.