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LOW AREA PROGRAMMABLE MEMORY BUILT-IN SELF-TEST (P-MBIST) FOR SMALL EMBEDDED RAM CORES

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AUTHOR'S DECLARATION

I declare that the work in the thesis was carried out in accordance with the regulations of Universiti Teknologi MARA. It is original and is the result of my own work, unless otherwise indicated or acknowledged as referenced work. This thesis has not been submitted to any other academic institution or non-academic institution for any degree of qualification.

I, hereby, acknowledge that I have been supplied with the Academic Rules and regulations for Post Graduate, Universiti Teknologi MARA, regulating the conduct of my study and research.

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ABSTRACT

As latest trend in designing processors and system-on-chips (SoCs) requires more RAMs than logics, these embedded RAMs contribute to the high percentage of yields for these processors and SoCs. To ensure high percentage of yield is achieved, a built-in self-test (BIST) is utilized to test these RAMs. The memory BIST applies various test algorithms such as MARCH tests to detect various RAM faults. Numerous design objectives such as programmability, low area overhead, at-speed/full-speed test and multiple RAMs target are proposed in the BIST designs. These objectives must be achieved to provide best fault detection in these embedded RAMs. A technique called clustering which is applied to other architectures such as VLIW processor and FPGA architecture is utilized in this study to achieve low area programmable memory BIST (P-MBIST). Three experiments are performed in this study. The first experiment is performed by clustering test patterns of RAMs under test. The second experiment deeply encodes the clusters of test patterns to improve the cluster technique to allow multiple test data types. The third experiment is performed to concurrently test an array of small embedded RAMs which is developed on a FPGA device. The simulation and synthesis tools used in these experiments are ModelSim, ALTERA's Quartus II and Synopsys Design Compiler. The FPGA implementation is performed on the Cyclone II FPGA device of ALTERA's DE2-70 board. It is justified that the cluster technique provides full-speed test and low area overhead for the programmable memory BIST controller. The proposed clustered FSM-based and microcode-based P-MBIST achieves around 15% and 32% of area reduction respectively. This area reduction is further improved in the proposed deep-encoded FSM-based and microcode-based P-MBIST where their areas are around 25% and 44% respectively. The lower and upper nibbles looping in the address generator proves that concurrent test of multiple RAMs target can be achieved.

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CHAPTER ONE

INTRODUCTION

1.1 BACKGROUND STUDY

The future trends in the processors and systems on chip (SoCs) are moving from logic and memory balanced chips to memory dominated chips in order to deal with the increasing application requirements. According to [1], the embedded memories are expected to utilize more than 83% of the chip area after 2008. Typically, embedded memories account approximately half the area of the microprocessor [4] and their density is continuously raising. They are scattered around the device (SoCs) rather than concentrated in one location [5]. As a result, the overall SoC yield is dominated by the memory yield. In order to achieve high memory yield, a thorough understanding of memory design, faults models and adequate tests strategies is a must.

Basically there are two types of memories: Random Access Memory (RAM) and Read Only Memory (ROM). RAM is the volatile memory where its contents are lost when it is powered off. There are two types of RAM: static and dynamic. Static RAM or commonly known as SRAM is built by transistors and data is stored using their architectural transistors. The dynamic RAM or commonly known as DRAM architecture comprises of a transistor and a capacitor and data is stored as the charge of the capacitor. The data in SRAM retains its value during power-on while the data in DRAM has to be periodically refreshed to be retained during the power-on. As for ROM, it is a non-volatile memory. Unlike RAM, its contents are kept after it is powered off. Examples of ROMs are programmable ROM (PROM), Erasable PROM (EPROM), Electrically Erasable PROM (EEPROM) and Flash.

More RAMs are embedded in today's processors and SoCs to accommodate wide range of computer applications such as gaming and Internet. These embedded RAMs use fault models to classify types of faults that may affect them during test. The RAM fault models are classified according to how the read/write operation is performed on the RAM cell arrays. Bit-oriented memories (BO-RAM) are the memories where the read/write operations are performed on the RAM cell arrays by