

RF oscillator Based on Passive RC Bandpass Filter

Mohd Azrul Aminur Rashid Bin Rofiee
Faculty of Electrical Engineering
Universiti Teknologi MARA
Shah Alam, 40450, Selangor, Malaysia
e-mail: aqua88_born@yahoo.com.my

Abstract—The purpose of this paper is to design a passive RC bandpass filter (BPF) based voltage-controlled-oscillator (VCO) operating at 2.5 GHz. A preferred type of an oscillator to operate in the GHz frequency range is either an LC oscillator or a ring oscillator. In fabrication, an LC oscillator involving high cost due to the inductors even it exhibits an excellent phase noise performance. On the other hand, ring oscillator resulting a cheap fabrication cost because it can be built with standard CMOS devices. However, it has a poor phase noise and jitter performance and is sensitive to power supply noise. This paper proposes an RC BPF-based oscillator. Its purpose is to close the performance of an LC oscillator than a ring oscillator, as a result to improve the phase noise performance. Furthermore, it can be fabricated in a standard CMOS process since there is no inductor. To prove the proposed concept, a RC BPF-based oscillator was designed with operating frequency of 2.5 GHz and phase noises -98.1 dBc/Hz at 1MHz offset frequency. The power consumption extracted from the simulation is 2.38 mW for 1.8 V supply voltage.

Keywords-component; *Bandpass filter, jitter, oscillator, passive filters, phase noise*

I. INTRODUCTION

Oscillators are important in many different types of electronic equipment. For example, a quartz watch uses a quartz oscillator to keep track of what time it is. An AM radio transmitter uses an oscillator to create the carrier wave for the station, and an AM radio receiver uses a special form of oscillator called a resonator to tune in a station. There are many application of oscillator to applied in electronic and communication field. Voltage-controlled-oscillator(VCO) is the type of oscillator whose oscillation frequency is controlled by a voltage input. The applied input voltage determines the instantaneous oscillation frequency. Consequently, modulating signals applied to control input may cause frequency modulation(FM) or phase modulation(PM). VCOs has a highly linear relation between applied voltage and frequency. VCOs may have sine and/or square wave outputs. Function generators are low-frequency oscillators which feature multiple waveforms, typically sine, square, and triangle waves. Analog phase-locked loops typically contain VCOs. High-frequency VCOs are usually used in phase-locked loops for radio receivers. In this paper, the VCOs was designed for the purpose of application in the phase-locked loops(PLL).

The most suitable oscillator type depends on the application example for the radio frequency(RF) communication systems, the LC oscillator is preferable due to its excellent

phase noise performance[1]. However, an inductor is expensive in CMOS fabrication because it takes a significant silicon area and it is not standard device. A thick copper is usually used in many modern CMOS processes instead of a standard aluminium to improve a Q-factor, which also affect to fabrication cost higher. The alternative way to give a lower fabrication cost is ring oscillator because it does not require an inductor. Additionally, ring oscillator yields wide frequency tuning ranges. However, compare to LC oscillator, the performance of ring oscillator is not good. Moreover, ring oscillator produce limit oscillate frequency by the number of stages as the total period is twice the sum of the stage delays. Typically three stages are the minimum number in ring oscillator for the phase sufficient to has unity gain. There have been several approaches to decrease the number of stages to increase the maximum oscillation frequency and decrease the power consumption[2]-[4]. In the other hand, if an active inductance is used, it still needs at least two stages, because the load is low pass and just contributing 90° phase.

This paper presents RC bandpass filter(BPF)-based oscillator. It provides sufficient phase shift with only one stage since the load is BPF. The frequency is less susceptible to power supply noise because the oscillation frequency is determined by a BPF made of passive component such as resistors and capacitors. A Wein-bridge [5],[6] oscillator is a classically oscillator that uses BPF as the load. However, this oscillator has limited oscillation frequency due to gain-bandwidth product of an opamp. So, as a result a Wein-bridge oscillator is not practical in GHz frequency ranges. To overcome this problem, an oscillator using an operational transconductance amplifier is proposed in this paper.

II. METHODOLOGY

This section will show the flow chart, block diagram and procedure of this project. All the theory and the background behind the BPF-based oscillator will be explained in detail in this section.

A. Flow Chart of the Project

The design step of the RC BPF oscillator is shown in Figure 1. The first step of design approach is research and gathering information. At this stage, research was undertaken by various means for example reading journal, technical paper, books and web pages about things that are related to purpose oscillator. The second stage is design the sketched oscillator in software LT-spice to simulate it. The third stage, all the parameter are determined to reach a desire oscillator for this proposed paper. The fourth stage is transient analysis is applied to observe the

output of oscillator as a function of time. The next stage is in term to achieve minimal noise and power consumption, the optimization of the oscillator is performed.

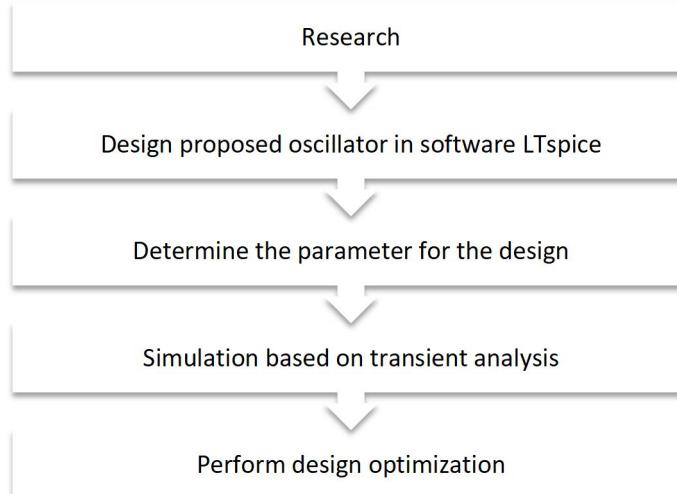


Figure 1. The design step of the RC BPF oscillator

B. Bakcground of BPF-Based Oscillator

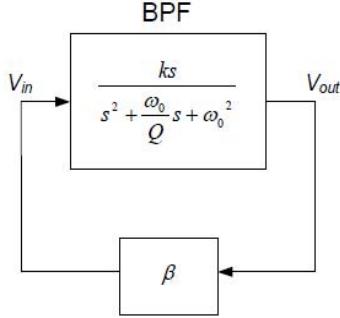


Figure 2:Block diagram of a BPF-based oscillator

Figure 2 shows the block diagram of a BPF-based oscillator. Positive feedback amplifier is attached together with a BPF to produce an oscillating signal(V_{out}). Assume BPF is a second order system and characterized by a coefficient k , a center frequency ω_0 and a quality-factor. The BPF has sufficient phase condition for oscillation which is it has one zero at DC and two pole;its phase response varies from $+90^\circ$ to -90° and crosses 0° at ω_0 . Initially,two poles are place at the left-half plane(LHP) and pushed toward right-half plane(RHP) by the positive feedback(regenerate feedback) with a loop gain β . Poles in a closed loop can be found by solving characteristic equation that is $s^2 + \omega_0/Q s + \omega_0^2$. The two poles are displaced to the RHP and sufficient to oscillate if β is large enough. The Q factor determine the minimum value of β . The frequency selectivity of the BPF is inversely proportional to Q ,indicating that high Q reduces the phase noise of an oscillator.[1].

C. Wein Bridge Oscillator

Figure 3 shows a conventional BPF-based oscillator block diagram of Wein Bridge Oscillator[5]. To have a positive

feedback,an Op-amp is used and its voltage gain is A_v . The oscillation condition A_v is greater than 3 and the oscillation frequency, ω_0 as $1/(RC)$.

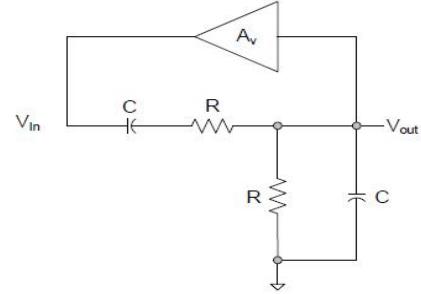


Figure 3:Block diagram of Wein-bridge oscillator

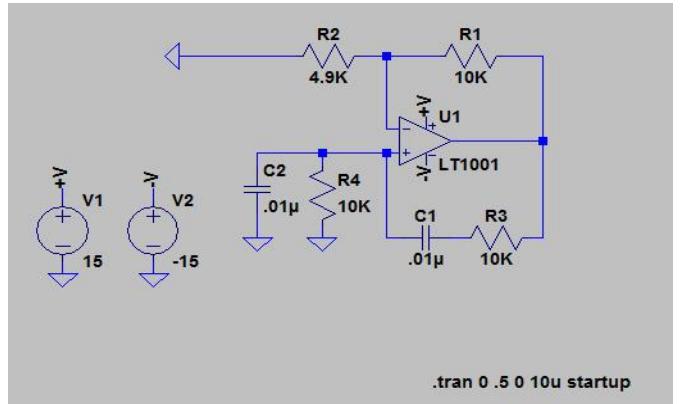


Figure 4:Schematic of Wein-bridge oscillator

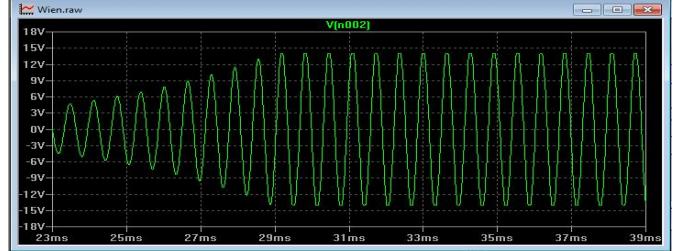


Figure 5:Transient response of Wein-bridge

Figure 4 shows Wein-Bridge oscillator design in LTspice and its output oscillation as shows in figure 5 in transient analysis. The circuit is design to produce 1.59 kHz with $R_3=R_4=10k$ and $C_1=C_2=0.01\mu F$. However, this approach is only valid at very low frequency of operation (<1% of the Op-amp bandwidth)[7]. Due to this limitation, the Wein-bridge oscillator is not suitable for high frequency.

D. An Oscillator using an Operational Transconductance Amplifier(OTA)

An oscillator using an operational transconductance amplifier(OTA) was proposed in[8] to overcome the frequency limitation by Wein-Bridge oscillator. It is possible to operate at higher frequencies since an OTA does not have a low impedance output stage and can be implemented as a simple structure. The oscillation frequency is sensitive to mismatch

between the two different feedbacks because this oscillator requires both negative and positive feedback. Figure 6(a) shows the block diagram of single-ended version of the proposed oscillator. On the other hand, Figure 6(b) shows an OTA with positive gain is easily designed by a fully differential structure. An RC BPF is used with a feedback through the single input OTA. A feedback in this proposed oscillator is gm .

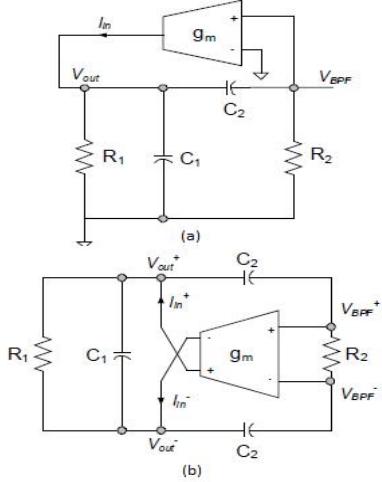


Figure 6: Block diagram of a proposed oscillator.(a)Single-ended version (b)Fully differential version

The open loop transfer function of the BPF produce equation

$$H(S) = \frac{V_{out}}{I_{in}} = \frac{\frac{1}{C1}s}{s^2 + \frac{1+C1/C2+R2/R1}{R2C1}s + \frac{1}{R1C1R2C2}} \quad (1)$$

To initially place the poles of closed loop at the RHP causing the oscillation to start is by the feedback through the OTA must be positive and the OTA gain(gm) should be large enough. A closed loop equation $Hcl(s)$ and a characteristic equation $D(s)$ are :

$$Hcl(s) = \frac{H(s)}{1-gmH(s)} = \frac{(1/C1)s}{D(s)} \quad (2)$$

$$D(s) = s^2 + \left(\frac{1+C1/C2+R2/R1}{R2C1} - \frac{gm}{C1} \right)s + \frac{1}{R1C1R2C2} \quad (3)$$

The BPF center frequency wo , and the minimum requirement for gm is set to has the oscillation frequency by this equation below

$$wo = \frac{1}{\sqrt{R1C1R2C2}} \quad , \quad gm > \frac{1+C1/C2+R2/R1}{R2} \quad (4)$$

The Q-factor, an important design parameter for the BPF-based oscillator, yields

$$Q = \frac{\sqrt{(C1/C2).(R2/R1)}}{1+C1/C2+R2/R1} \quad (5)$$

For design convenient, resistors and capacitors are chosen as $R2=R2=R$ and $C1=C2=C$, then

$$wo = 1/(RC) \quad , \quad gm > 3/R \quad , \quad Q=1/3 \quad (6)$$

From (5), when both $R2/R1$ and $C1/C2$ are infinite, it can be concluded that the maximum achievable Q-factor is 0.5. The total harmonic distortion (THD) and phase noise performance of the oscillator are improved [9]-[10] as Q-factor is increased. When Leeson's model [10] is applied, the phase noise and moderate frequency is improved by 3.5dB from Q of 0.3333 to 0.5.

$$L\{\Delta w\} = 10 \cdot \log \left(\left[1 + \frac{1}{4Q^2} \left(\frac{wo}{\Delta w} \right)^2 \right] \frac{FkT}{P} \right) \quad (7)$$

Where F is noise factor, k is Boltzman constant, T is absolute temperature and P is a carrier power.

Phase noise of the proposed oscillator will not be able to reach of an LC oscillator due to the limitation of a low Q-factor. However there is little difference with ring oscillator.

E. Circuit Implementation of The RC BPF-based Oscillator

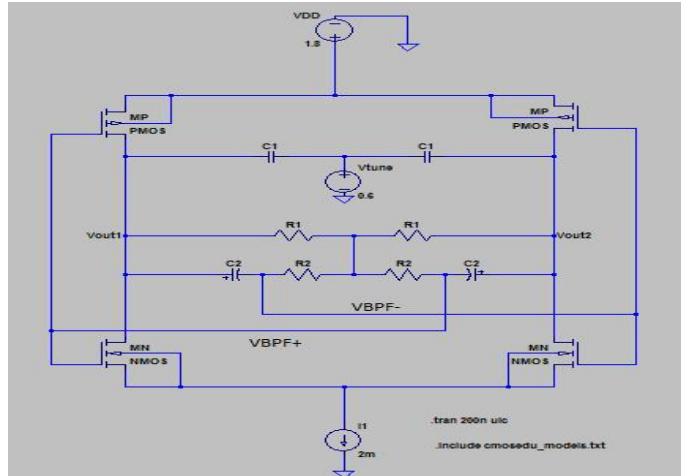


Figure 7:Schematic of the proposed fully differential RC BPF-based oscillator

Figure 7 shows the schematic of proposed oscillator which is $R1, R2, C1$ and $C2$ form a BPF, and transistors MN and MP take the voltage at the output of the BPF ($VBPF+$ and $VBPF-$) and transform these voltages to current which are fed back to the BPF. A fully differential circuit is used for positive feedback. The oscillator output normally taken from BPF output ($VBPF+$ and $VBPF-$) but the amplitude is low, so output is taken from $Vout1$ and $Vout2$ because it has larger amplitude. The common-mode voltage of $Vout1$ and $Vout2$ is sensed by $R1$, and is used to bias gate voltages of MN and MP through $R2$. The oscillator starts oscillate once gm of MN and MP are

set larger than the minimum requirement given by (4) and the oscillation frequency is fixed at ω_0 as described in (4).

Parasitic effects give the oscillation frequency deviates from the ideal value. Two parasitic effect should be considered in this oscillator. First, parasitic capacitance (C_{db} (capacitance drain to body of MP and MN)) and the finite output resistance (R_{out} of MN and MP) at V_{out+} and V_{out-} should be considered. Fortunately, C_1 and R_1 can absorb this parasitic and they do not generate additional poles or zeros. The second parasitic effect is the input capacitance (C_{gs} (capacitance gate to source)) of MN and MP, which are V_1 is a virtual ac ground.

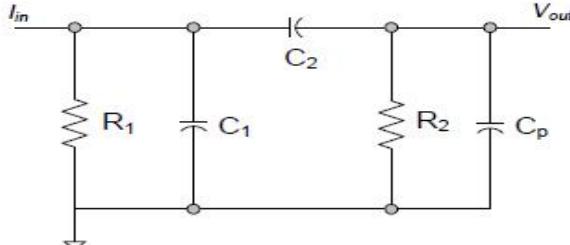


Figure 8:RC BPF with a parasitic capacitance C_p

Figure 8 shows if a parasitic capacitance C_p is included and becomes

$$H(s) = \frac{\frac{1}{C_1 k p} s}{s^2 + \frac{1 + R_2/R_1 + (C_1/C_2)(1 + C_p/C_1)}{R_2 C_1 k p} s + \frac{1}{R_1 C_1 R_2 C_2 k p}} \quad (8)$$

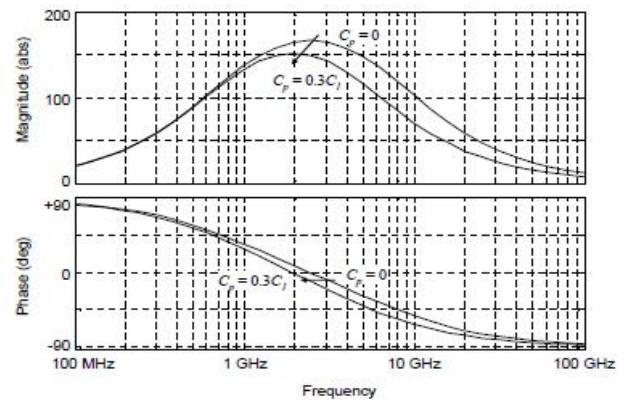
Where $k p = 1 + (C_p/C_1)(1 + C_1/C_2)$ and C_p represent all parasitic capacitance connected to the BPF output. From equation (8) ,the oscillating frequency,Q-factor and g_m become

$$\omega_0^2 = \frac{1}{R_1 C_1 R_2 C_2 (1 + (C_p/C_1)(1 + C_1/C_2))} \quad (9)$$

$$g_m = \frac{1 + R_2/R_1 + (C_1/C_2)(1 + C_p/C_1)}{R_2} \quad (9)$$

$$Q = \frac{\sqrt{(C_1/C_2)(R_2/R_1)}}{1 + R_2/R_1 + (C_1/C_2)(1 + C_p/C_1)} \times \sqrt{1 + (C_p/C_1)(1 + C_1/C_2)}$$

Equations (8) consider that if $C_p/C_1 \ll 1$ and $C_p/C_2 \ll 1$,then the effect of C_p can be neglected. The size of MN and MP is proportional to the C_p ,as g_m and ω_0 are increased, C_p is increased and C_1 should be decreased,for this reason, C_p/C_1 cennot be neglected anymore. To evaluate the deviation of ω_0 and g_m ,suppose that a BPF is designed with $R_1=R_2=300$ and $C_1=C_2=210fF$ so that ω_0 is normally 2.5GHz. Figure 9 depicts the deviation of the transfer function when $C_p=63fF$ (30% of C_1 is considered. Oscillation frequency, ω_0 moves 20%(from 2.45GHz to 1.94 GHz) and g_m increased 10%(from 6 mA/V to 6.6 mA/V).



(a)

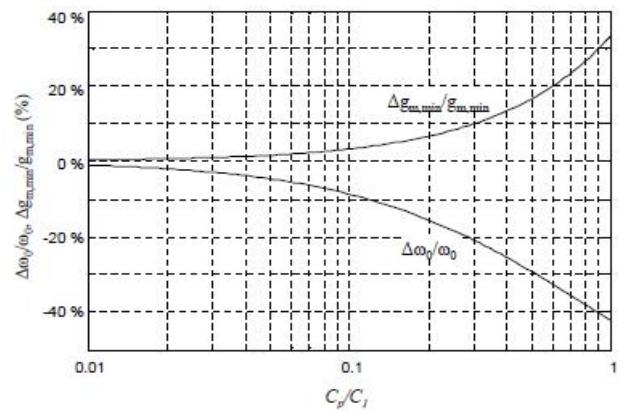


Figure 9:BPF performance deviation due to C_p (a)Transfer function(b) $\Delta\omega_0$ and $\Delta g_m, \min$

In figure 9(b) plots the changes in ω_0 and g_m as C_p/C_1 varies from 1% to 100%. When $C_p/C_1=10\%$, ω_0 and g_m change by 8% and 4% respectively.

F. A Design Optimization for the Minimal Noise and Power Consumption

The objective of the section is to describe an optimal design of resistors and capacitors of the band pass filter in terms of the minimum noise and power consumption. Consider a linearized,open-loop model of the proposed oscillator shwn in Figure 10.

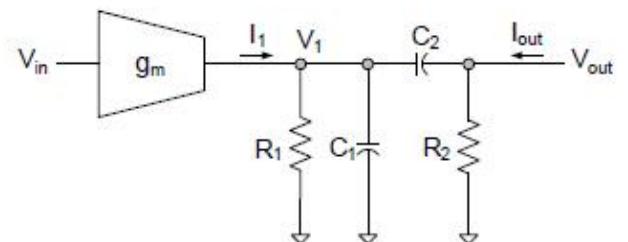


Figure 10:Block diagram of the linearized open-loop model of the proposed oscillator

The key design parameters are resistor and capacitors:

$$k_R = \frac{R}{R_1} = \frac{R^2}{R}, k_C = \frac{C_1}{C} = \frac{C}{C_2} \quad (10)$$

Where R and C are design variables determined by the oscillation frequency. Note that, once R and C are fixed, the oscillation frequency is not changed by varying k_R and k_C . Hence, the open-loop transfer function is given by

$$H(s) = \frac{V_{out}(s)}{V_{in}(s)} = \frac{gm \frac{1}{k_C C} s}{s^2 + \frac{1+k_R^2+k_C^2}{k_R k_C R C} s + \left(\frac{1}{R C}\right)^2} \quad (11)$$

From equation (11), the oscillation frequency ω_0 , a Q-factor and the minimum required gm are calculated as

$$\omega_0 = \frac{1}{RC}, Q = \frac{k_R k_C}{1+k_R^2+k_C^2}, gm = \frac{1+k_R^2+k_C^2}{k_R R} \quad (12)$$

Note that ω_0 is determined by R and C , not by k_R and k_C . In figure 11, a current injected to node V_{out} (I_{out}) can be referred to the current injected to node V_1 (I_1) at ω_0 with the following transfer function:

$$|\frac{I_1}{I_{out}}(j\omega_0)|^2 = (1+k_C^2)^2 + (k_R k_C)^2 \quad (13)$$

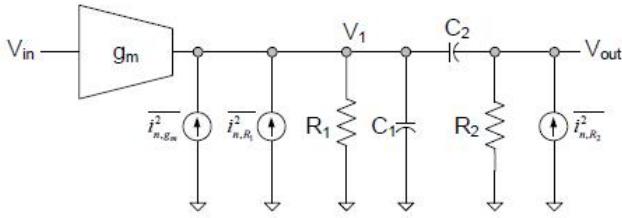


Figure 11: Individual noise current source in Figure 10

Figure 11 shows various current source $I_{n,R2}^2$ is injected to the V_{out} node while $I_{n,R1}^2$ and $I_{n,gm}^2$ are injected to the V_1 node, and using equation (14), $I_{n,R2}^2$ associated with R_2 can be referred to the V_1 node. Assuming $gm = gm_{min}$, the total noise current at the V_1 node is

$$I_{1,total}^2 = \frac{4kT}{R_1} + 4kT\gamma gm + \frac{4kT}{R_2} ((1+k_C^2)^2 + (k_R k_C)^2) = \frac{4kT}{R} (1+k_C^2 + \gamma) (k_R + \frac{1+k_C^2}{k_C}) \quad (14)$$

Where γ is the factor to be $2/3$ for long-channel transistors and larger value for a short-channel transistor. A total input referred noise voltage can be calculated from equation (12) and (14)

$$V_{in,total}^2 = \frac{I_1^2}{gm_{min}^2} = \frac{4kTRk_R^2}{(1+k_R^2+k_C^2)^2} (1+k_C^2 + \gamma) (k_R + \frac{1+k_C^2}{k_R}) \quad (15)$$

A noise shaping function in the linearized VCO model at frequencies close to ω_0 is determined in [1]

$$|\frac{V_{out}}{V_{in}}[j(\omega_0 + \Delta\omega)]|^2 = \frac{1}{4Q^2} \left(\frac{\omega_0}{\Delta\omega}\right)^2 \quad (16)$$

As a consequence, the total output noise voltage can be calculated using (12), (13) and (16).

$$|V_{out}[j(\omega_0 + \Delta\omega)]|^2 = \frac{kTR}{k_C^2} (1+k_C^2 + \gamma) \left(k_R + \frac{1+k_C^2}{k_R}\right) \left(\frac{\omega_0}{\Delta\omega}\right)^2 \quad (17)$$

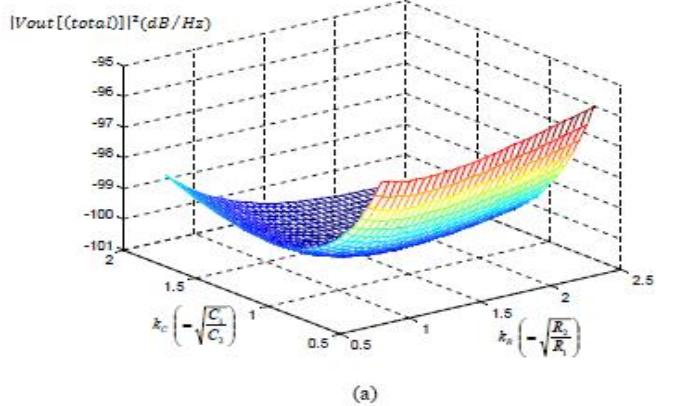
Figure 12 shows a 3-D plot of total output noise voltage and gm in equation (12) when k_R and k_C are varied. It should be considered that both gm and equation (17) reach their minimum values with following condition:

$$k_R^2 = 1 + k_C^2 \quad (18)$$

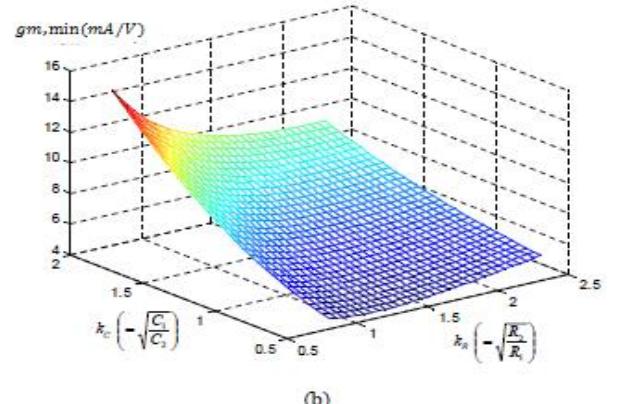
Applying equation (18) to (17) and (12) simplifies them to one variable equation (k_C) as,

$$|V_{out}[j(\omega_0 + \Delta\omega)]|^2 = \frac{kTR}{k_C^2} (1+k_C^2 + \gamma) \cdot (2\sqrt{1+k_C^2} \left(\frac{\omega_0}{\Delta\omega}\right)^2) \quad (19)$$

$$gm, min = \frac{2k_C^2}{R\sqrt{1+k_C^2}}$$



(a)



(b)

Figure 12: VCO performance versus k_R and k_C (a) Total output noise voltage (b) gm_{min}

Figure 13 shows equation (19) versus k_C with an oscillating frequency of 2.5GHz and an offset frequency of 1MHz. From (18) to (19), a total output noise voltage becomes minimal when $k_C=1.68$ and $k_R=1.96$ and is rapidly increased when k_C is less than 1. Meanwhile, gm is monotonically increased as k_C is increased. Therefore, a design trade-off can be made and, the optimal design can be considered as $k_C=1$ and $k_R = \sqrt{2}$ implying $C1=C2$ and $R2=2R1$.

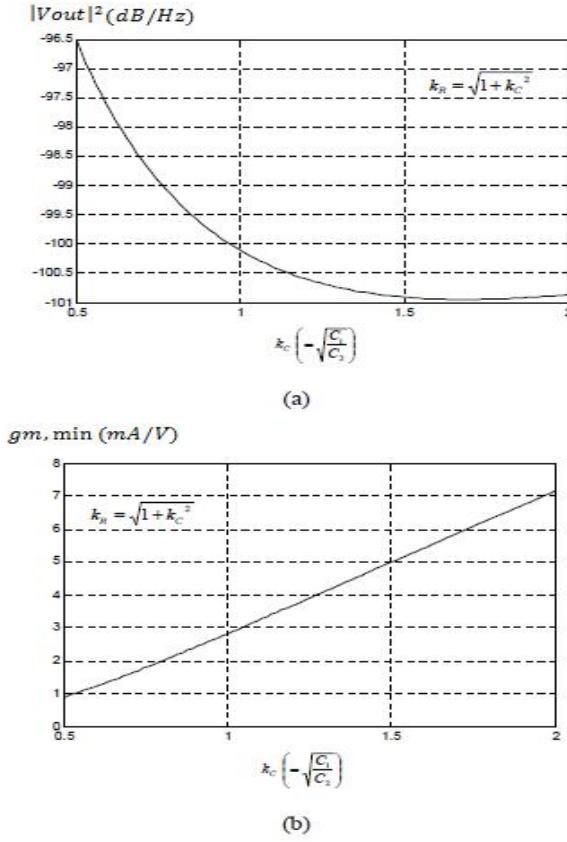


Figure 13: VCO performance versus k_C when k_R is optimized. (a) Total output noise. (b) gm_{min}

A design optimization has been performed to achieve minimal noise and power consumption. The optimal ratio of resistors and capacitors has been derived as $R2/R1 = C1/C2 + 1$. When this condition is met, the design trade-off between a total output noise voltage ($|Vout|^2$) and gm can be made by adjusting a capacitor ratio $k_C (= C1/C2)$. ($|Vout|^2$) rapidly increases when $k_C < 1$, while gm monotonically increased as k_C is increased. Although the optimal condition, $R2/R1 = C1/C2 + 1$, indicates the optimal design for ideal components with $Cp=0$, the actual ratio will significantly differ to account for non zero Cp .

III SIMULATION RESULTS AND DISCUSSIONS

The oscillator RC BPF-based oscillator in this paper is designed using $0.13\mu\text{m}$ CMOS technology. This oscillator is supplied with 1.8V and the current mirror is used to provide bias current to the circuit. In actual design, Cp is related to transistor sizes. In this paper, Cp was measured as 40fF. Given

Cp as 40fF and assuming $R1=R2 = 300$ and both capacitors are same ($C1=C2=C$), a required C for 2.5GHz of an oscillating frequency is calculated using

$$(2\pi \times 2.5 \times 10^9)^2 = \frac{1}{300^2 C^2 (1 + 2x \left(\frac{40 \times 10^{-15}}{C} \right))} \quad (20)$$

Solving (21) yields $C=176\text{fF}$ that is quite practical to accurately implement in this process. Note that if Cp is not considered, the required C for 2.5GHz is 212fF. The schematic shown in figure 14 is designed base on this requirement including parasitic capacitor using LTspice software which is Cp was measured as 40fF.

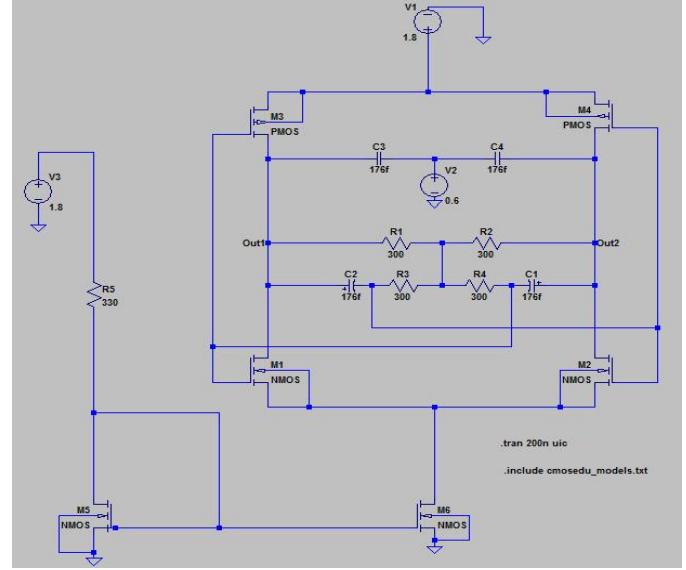


Figure 14: Schematic of RC BPF-based oscillator (parasitic capacitance Cp include)

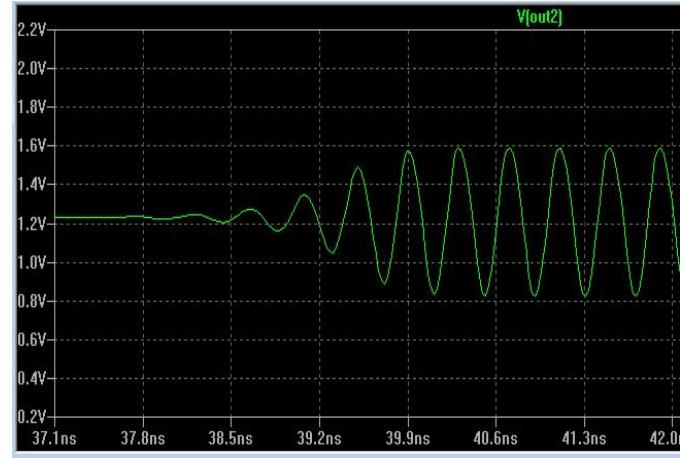


Figure 15: Transient response of proposed oscillator

Figure 15 shows the transient response for RC BPF-based oscillator with oscillation frequency 2.5 GHz with the duration of period is 0.4ns. To view the frequency spectrum of this signal, FFT(Fast Fourier Transform) simulation is applied to determine the fundamental oscillating frequency 2.5 GHz as shown in figure 16.

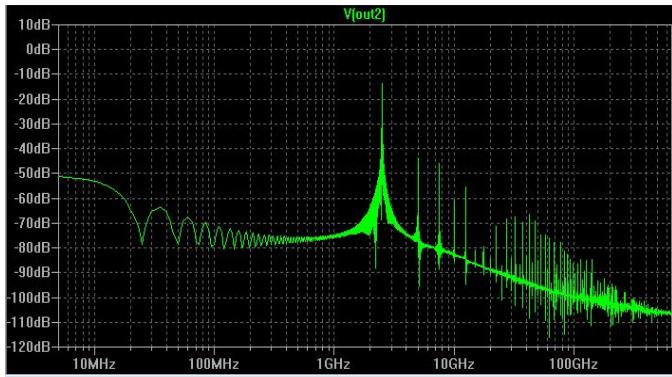


Figure 16:Frequency spectrum in FFT(Fast Fourier Trasform)

Power consumption is important consideration in designing an oscillator. Figure 17 shows proposed oscillator gives 2.73 mW for power consumption. Another important consideration in term to have better oscillator is phase noise. At 1 MHz offset frequency,- 96.2 dBc/Hz of phase noise is measured as shown in figure 18.

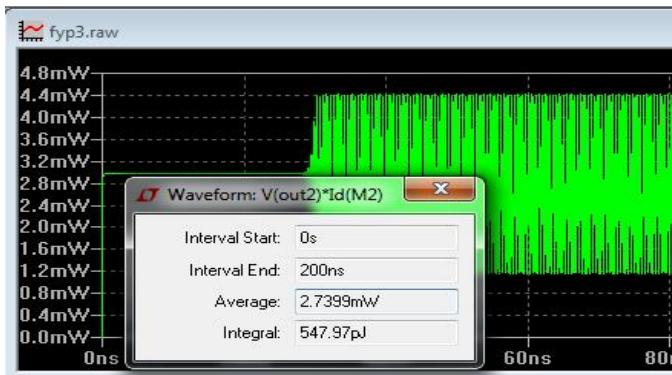


Figure 17 :Power consumption of proposed oscillator

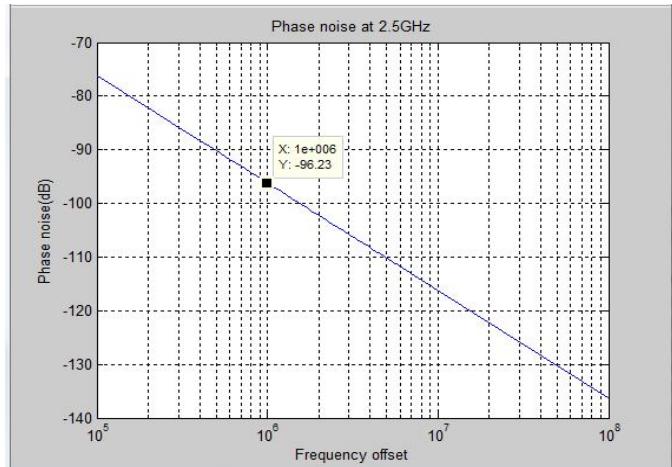


Figure 18:Phase noise at 2.5GHz(frequency offset@ 1MHz gives -96.2 dBc/Hz phase noise)

Design optimazation is achieved by implying $C1=C2$ and $R2=2R1$ as dicussed previous section. Figure 19 shows a schematic of propose oscillator with parameter both of capacitors and resistors is adjusting to optimal design which is $C1=C2=160fF$ and $400 \Omega=2(200\Omega)$.

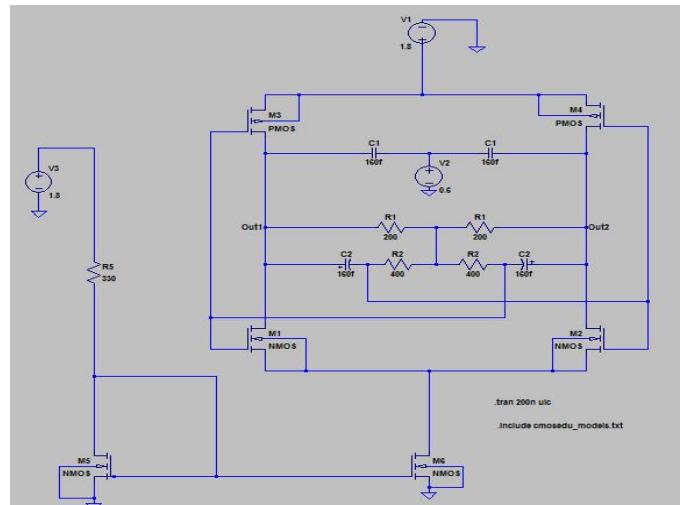


Figure 19:Schematic of proposed oscillator(after optimization)

The oscillator is designed to have a center frequency $f_0=2.5\text{GHz}$ with the Q factor of BPF is designed to be 0.44 compare to previous schematic before optimize with the Q factor 0.33.

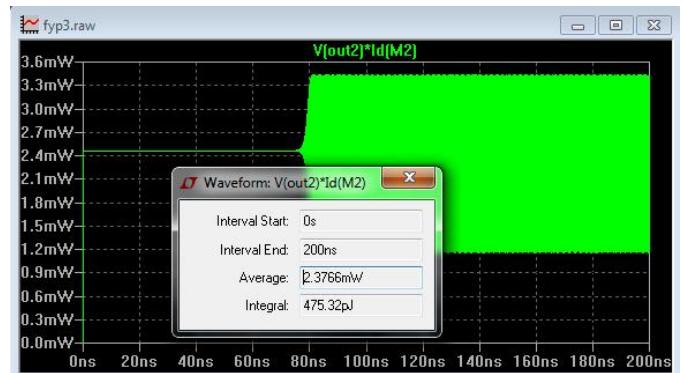


Figure 20:Power consumption(after optimization)

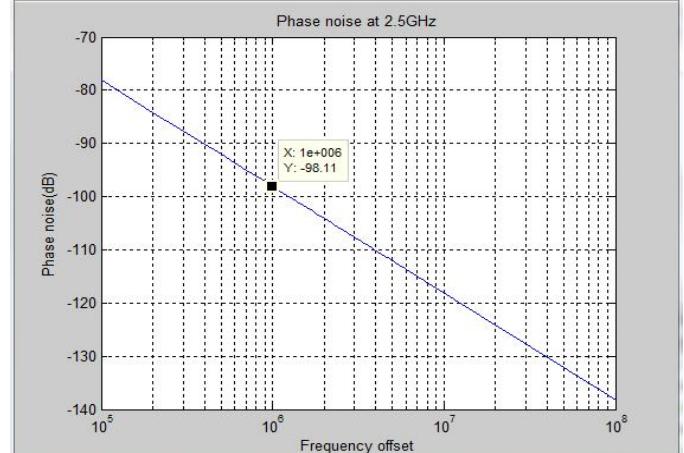


Figure 21:Phase noise at 2.5GHz(frequency offset @ 1MHz gives -98.11 dBc/Hz after optimization)

Two main consideration in optimization design are power consumption and phase noise performance. Before

optimization, the value of this two consideration are 2.74 mW for power consumption and -96.2 dBc/Hz for phase noise. After optimization, power consumption has been reduced to 2.38 mW and phase noise performance has improved to -98.11 dBc/Hz. The objective an optimal design for this purpose oscillator has achieved in terms to minimum the noise and power consumption. Table I shows summary of result before and after the optimization design.

Table I:Summary of result before and after optimization

	Before optimization	After optimization
Frequency (GHz)	2.5	2.5
Power consumption (mW)	2.74	2.38
Phase noise@ 1 MHz offset (dBc/Hz)	-96.2	-98.11

In Figure 22, the oscillating frequency was tuned by the control voltage from 0 to 1.2 V and the covered frequency range was 2.23 ~ 2.51 GHz.

Table II compare the performance of the proposed oscillator with other published solutions running at frequency around 2.5GHz. A normalized phase noise has been typically defined as a figure of merit(FOM) for oscillator[11].

$$FOM = \mathcal{L}(\Delta\omega) + 10\log \left[\left(\frac{\Delta f}{f_0} \right)^2 \left(\frac{P_{vco}}{mW} \right) \right] \quad (11)$$

Where P_{vco} is the total power consumption in mW and Δf is the offset frequency where the phase noise was measured. The proposed oscillator shows a good phase noise and small power consumption resulting in a FOM of -162 dB, better than the previously reported oscillator in Table II.

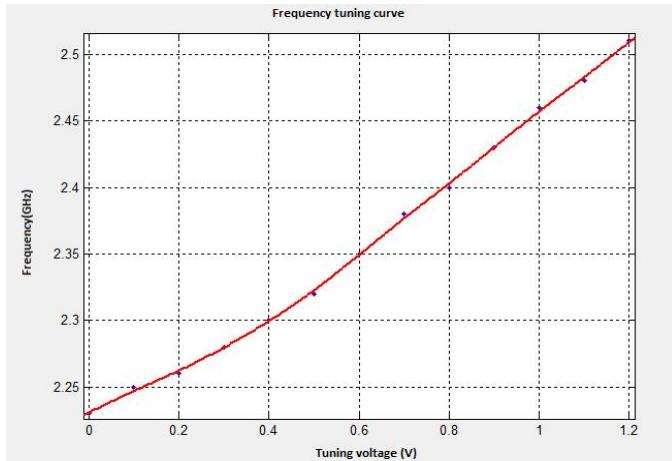


Figure 22:Frequency tuning curve

Table II:Performance summary and comparison with other published solutions

	This work	[12]	[13]	[14]	[15]
Frequency (GHz)	2.5	2.5	2	2.4	2.45
Power (mW)	2.38	10	0.7	1.5	19.2
Phase noise @1MHz offset(dBc/Hz)	-98.11	-80	-90	-97	-96
Type	RC BPF	2-stg. Ring	2-stg. Ring	3-stg. Ring	2-stg Ring
Process	0.13um CMOS	0.35um CMOS	0.18um CMOS	0.35um CMOS	0.28um CMOS
FOM(dB)	-162	-124	-157	-153	-151

IV. CONCLUSION

This paper has investigated an RC BPF-based oscillator appropriate for RF application. A prototype oscillator using simulation operating at 2.5GHz has been designed in LTspice, and measurement results have validated the proposed idea. The phase noise is worse than an LC oscillator due to the low Q-factor of the proposed BPF-oscillator, but comparable to a ring oscillator. Furthermore, the silicon area is essentially smaller than commensurate LC oscillator by avoiding the use inductors.

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