Simulation of Drain Induced Barrier Lowering (DIBL) in Metal Oxide Semiconductor Field Effect Transistor (MOSFET)

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Abstract—**This paper shows Simulation of Drain Induced Barrier Lowering (DIBL) in Metal Oxide Semiconductor Field Effect Transistor (MOSFET)". The research and study on this is investigated. Using software from SILVACO International, the simulation of the N-channel metal oxide semiconductor (NMOS) can be studied and the study is about DIBL due to short channel. SILVACO technology computer-aided design (TCAD) software is use to do the simulation and to obtain all the results needed. The virtually fabrication of NMOS is done using ATHENA module meanwhile for electrical characterizations of NMOS is done using ATLAS module. Using this software, the structure of MOSFET and I-V curve can be plotted through the TONYPLOT. In this study, the drain voltage, V_D and channel length, L act as the main roles in the results. Therefore, to see the role of drain voltage on DIBL, five different values of drain voltage, V_D which are 0.1V, 0.2V, 0.3V, 0.4V and 0.5V are used. Meanwhile, for channel length, L, the values used are 0.20μm, 0.30μm, 0.40μm and 0.50μm. From drain current, I_D versus gate voltage, V_G (I-V) curve, the value of DIBL is obtained and analyzed to complete the analysis of DIBL. When the drain voltage, V_D increasing, the potential barrier in the channel decreasing which leads to DIBL. As the voltage drain, V_D is increasing, and the barrier height is decreasing while the drain current, I_D is increasing. This project do achieved the objectives of the project.**

Keywords-DIBL, SILVACO TCAD, NMOS, TONYPLOT

I. INTRODUCTION

MOSFET is a device which is used to amplify or to switch any kind of electronic signals. Nowadays, we can see that MOSFET technology is one of the most commonly used semiconductor technique, and had become one of the elements in the integrated circuit technology. The power consumptions in integrated circuits can be reduced as MOSFET's has good performance which enables the reduction.

A MOSFET has two regions which are mainly named as the source and drain. Both regions are heavily doped and these are implanted in a substrate, which is doped the other way. The current will finally flow at the gap between the source and drain regions, which spans the substrate. A layer of insulating oxide is placed over this gap, which is well known as the channel. Moreover, on top of that is a gate contact and it is usually made of polysilicon. Figure 1 shows the MOSFET structure.

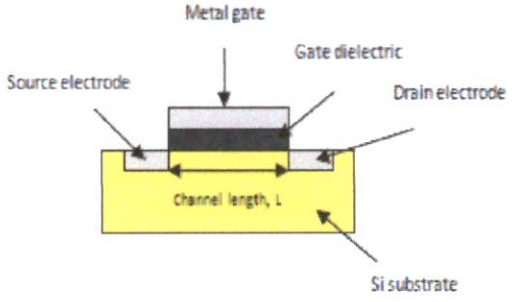

Figure 1: MOSFET Structure

The basic principle MOSFET is that the gate voltage, V_G controlled the source to drain current, I_{SD}. The electric field induces charge in the semiconductor at the semiconductor oxide interface that makes the MOSFET is a voltage controlled current source [1].

MOSFET comes in four types such as N-channel or P-channel and enhancement or depletion mode. The number of carriers increases according to the gate voltage, V_G in enhancement mode. Depletion mode acts by removing or depleting the carriers of the current from the channel [1]. Meanwhile for P-channel, a hole is induced in the n-type semiconductor by negative charges on the gate [1]. In this paper, it is more concentrate on the NMOS.

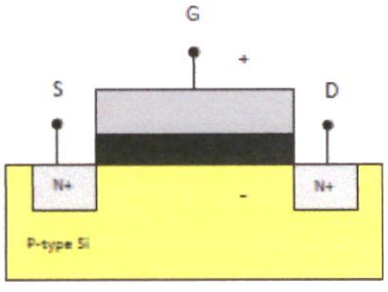

Figure 2: N-channel Si MOSFET

In Figure 2, by positive charges on the gate region, an electron is induced in the P-type semiconductor. As the source and drain are n+ regions and the body is a p region, the MOSFET is a n-channel type. The N-channel is much more commonly used on its own as a discrete device, eventhough both types, the N-channel and P-channel are widely used in integrated circuits.

II. LITERATURE REVIEW

MOSFET device is considered to be short channel when channel length, L is the same order of magnitude as the depletion-layer widths of the source and drain junction. As the channel length, L is reduced to increase the operation speed and number of components per chip, the short-channel effects arise [2]. There are five particular short channel effects occurs in the device such as DIBL and punch-through, surface scattering, velocity saturation, impact ionization and hot electrons. However, in this paper, the main focus is on the DIBL.

DIBL is a secondary effect in MOSFETs which referring originally to a reduction of threshold voltage, V_{TH} of the transistor at higher drain voltage, V_D. DIBL effect occurs in devices where only the gate length is reduced without properly scaling in the other dimensions [3]. As MOS devices are scaling down aggressively, DIBL effect is increasing [4]. However, investigation of the effect of increasing DIBL is lacking in literature [4].

DIBL is one of the most important short channel effects for devices such as VLSI MOSFET and DIBL in NMOS devices has been widely studied. DIBL is also one of the limitations in MOS technology due to the reduced channel length, L. As voltage drain, V_D increases, threshold voltage, V_{TH} decreases hence drain current, I_D increases.

As the channel length, L decreased, DIBL caused threshold voltage shift to first increased with increasing of substrate bias, and then decreased as the channel length decreased further away [5,10]. By an electron from the source, S on its way to the drain, D, the barrier to be surmounted is reduces as the channel length, L decreases. This can be shown in the Figure 3 below.

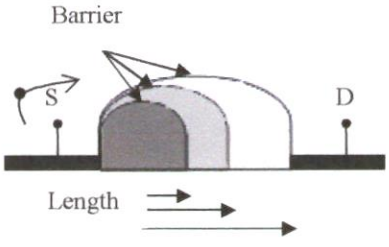

Figure 3: MOSFET Structure

SILVACO TCAD products that were used were ATHENA and ATLAS. ATHENA module is a process simulation product. It can develop and optimizes the semiconductor manufacturing processes.

ATHENA module can be manipulated well in the study of downscaling process as it can give speed edge and more economical to the traditional way of doing things [7]. ATHENA provides a platform for simulating ion implantation, diffusion, etching, deposition, lithography, and oxidation of semiconductor materials [5].

Meanwhile, ATLAS is a device simulation product. It provides a physics-based, modular, and extensible platform to analyze DC, AC, and time domain responses for all semiconductor based technologies in 2 dimensions and 3 dimensions [5]. It also can simulate the optical, electrical characteristics, and thermal behaviors of semiconductor devices. The simulations provide the opportunity to study the effect of different device parameters on the overall device performance [7].

III. METHODOLOGY

A. Flowchart

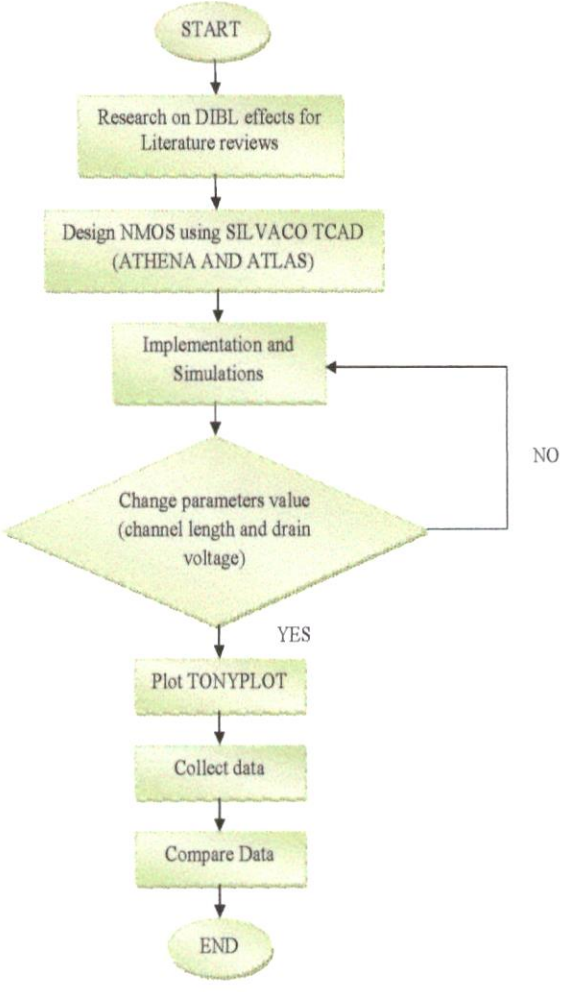

Figure 4: Flowchart of the flow of the project

Figure 4 shows the flowchart of the flow of the project. These project starts with the research on DIBL for Literature reviews writing. All these things are studied and understand carefully. After the research, the implementation and simulation of NMOS using SILVACO TCAD software, from ATHENA and ATLAS module are done. ATHENA module has to be done first then later continue with the ATLAS module.

There are two parameters changed which are channel length, L and drain voltage, V_D. The values used for channel length are 0.20µm, 0.30µm, 0.40µm and 0.50µm. Meanwhile, for drain voltage, the values are 0.1V, 0.2V, 0.3V, 0.4V and 0.5V. The values are the decision that has to be executing one by one. Once the decision is done, the TONYPLOT is plotted.

The obtained data's are collected once the implementation and simulation by both modules is done. The values obtained from the TONYPLOT (I-V curve) are recorded in table form. Then, all the data's are compared and analyzed for the project results.

IV. EXPERIMENTAL DETAILS

A. Device Details

The NMOS used in this paper were designed and fabricated by SILVACO TCAD. The orientation of the wafer is 100 and the substrate is p type, as indicated by a phosphorous concentration of ~1 x 10^{14} cm^{-3}. NMOS is fabricated in a p-type substrate of doping ~8 x 10^{12} cm^{-3}. The test devices had been tested with four different values of channel lengths, L which is 0.20µm, 0.30µm, 0.40µm and 0.50µm. The quantity of hydrochloric acid (HCL) used was 3% while the temperature was 1000°C. Also, the drain voltage, V_D is varied from 0.1V to 0.5V.

B. Equation

Effectively, DIBL leads to a reduction of threshold voltage, V_{TH} with the increasing of drain to source bias, V_{DS} through modulation or reduction of the potential barrier for carrier flow from source to drain by V_{DS} [8].

DIBL is quantify by R, and it is defined as the threshold-voltage shift, δV_{TH} (DIBL) divided by the drain voltage variation ΔV which is shown as the equation (1) below [8];

$$R = \frac{\delta V_{TH}(DIBL)}{\delta V_{DS}} = \frac{V_{TH}(V_{DS2}) - V_{TH}(V_{DS1})}{V_{DS2} - V_{DS1}} \quad (1)$$

with the threshold voltage, V_{TH} also known as as the gate voltage, V_G required for the fixed drain current, I_D [8]. The threshold voltage, V_{TH} (V_{DS2}) is measured at a supply voltage at the high drain voltage, V_D while threshold voltage, V_{TH} (V_{DS1}) measured at a very low drain voltage, V_D. V_{DS2} is the supply voltage at the high drain voltage and V_{DS1} is the low drain voltage.

V. RESULTS AND DISCUSSION

All simulation processes and the results were obtained by using SILVACO TCAD tools. From this software, it simulated NMOS device by using ATHENA and ATLAS. By using this software, the structure of NMOS and I-V curve required are obtained and plotted through the TONYPLOT.

From the results obtained, the DIBL characteristic is very sensitive to the channel length, L so that the measured minimum length is reasonable and cannot be equal or less than 0.10µm. This can be shown in Figure 5 where channel length used is 0.10µm and the structure does not turn out to be a perfect device. The depletion region surrounding the source and drain diffusions to approach with one another as the channel length decreases.

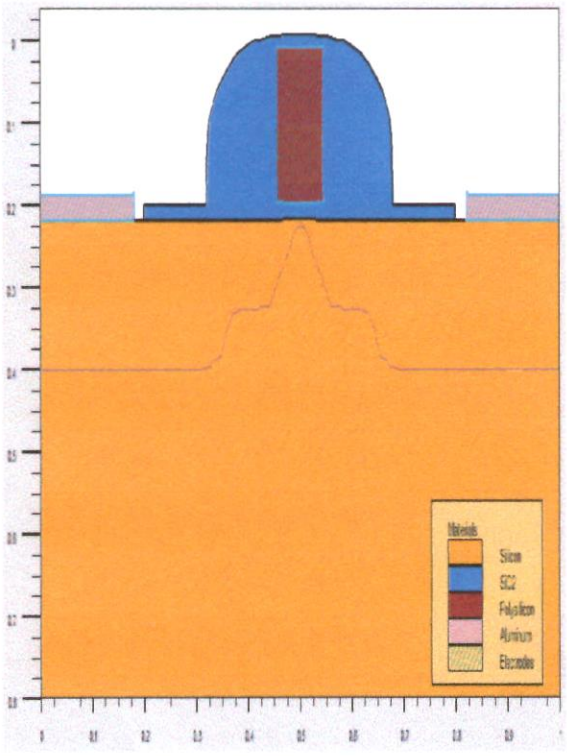

Figure 5: NMOS structure when channel length, L=0.10µm

In this paper, there are four different values of channel length, L used to do the comparisons between the structures and I-V curves. The values are 0.20µm, 0.30µm, 0.40µm and 0.50µm which are as shown in the in Figure 6 (a), (b), (c) and (d).

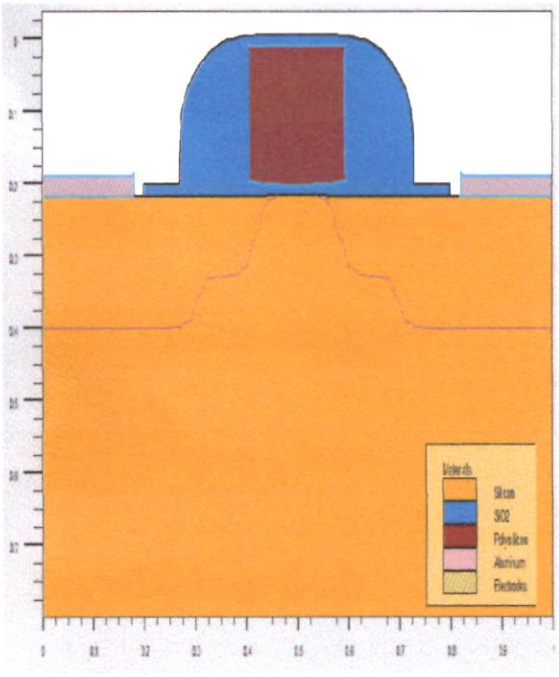

Figure 6: (a) NMOS structure when channel length, L=0.20μm

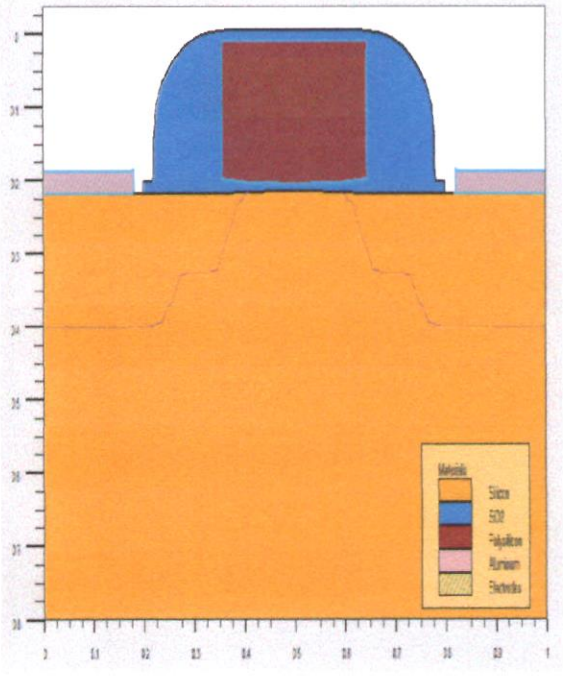

Figure 6: (b) NMOS structure when channel length, L=0.30μm

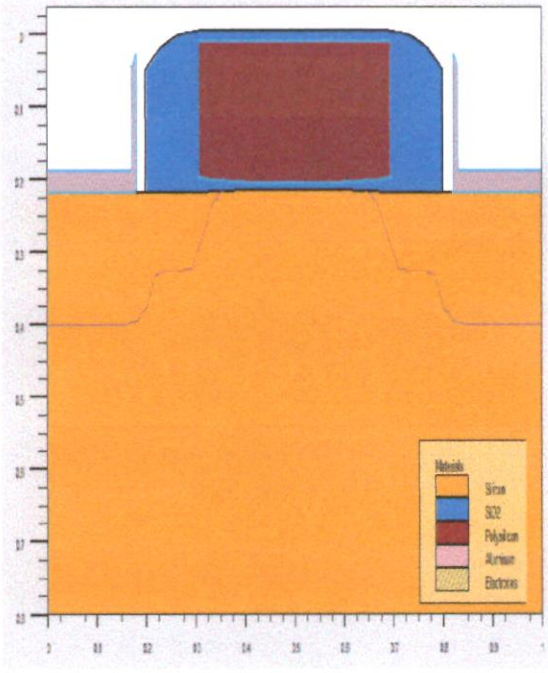

Figure 6: (c) NMOS structure when channel length, L=0.40μm

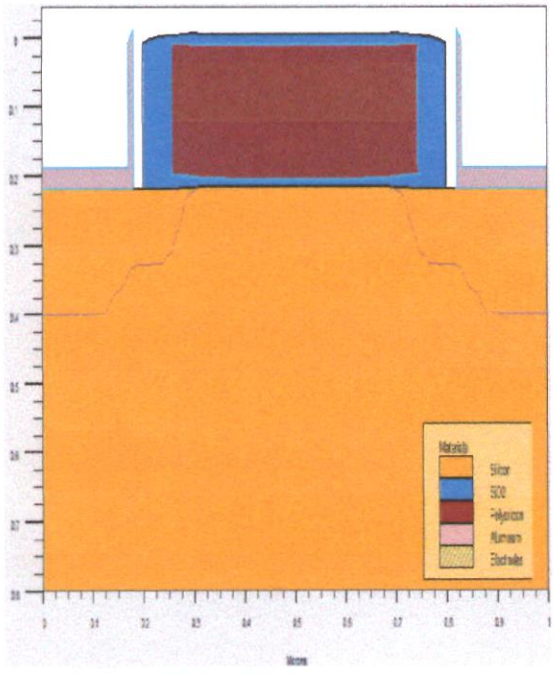

Figure 6: (d) NMOS structure when channel length, L=0.50μm

Figure 6 (a), (b), (c) and (d) show the NMOS structures with different channel lengths and without the contours. The structures are different from one another.

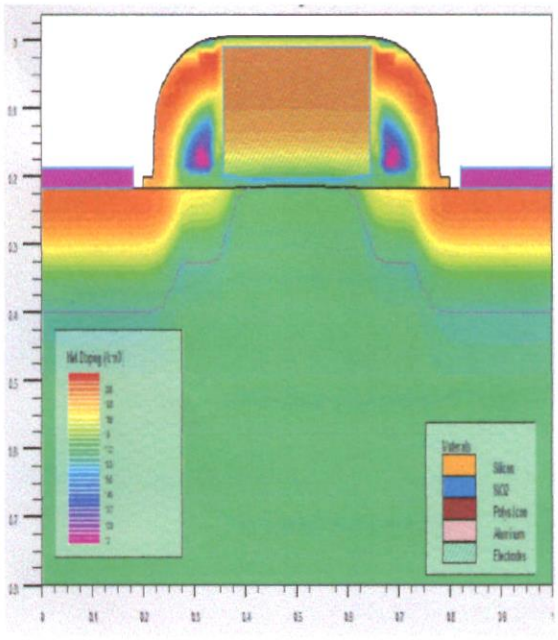

Figure 7: NMOS structure with its contours when channel length, L=0.30μm

Meanwhile Figure 7 shows the structure with the contours where the values of net doping can be seen and shows where is highly doped and lightly doped.

From the structure itself, the barrier lowering can be seen and the channel length became shorter as the value of the length used is increased. In short channel, the source and drain come closer, the horizontal field starts effecting thus lowering the barrier in the channel. At first, the structure device has only had one side, which is the source side. Then, to have the complete structure of NMOS, the previous one-sided structure is mirrored.

Next, the tables below shows the comparison of the values and data obtained during the simulations are done for V_D, gate bias and I_D when the 4 different channel lengths, L such as 0.20μm, 0.30μm, 0.40μm and 0.50μm are used.

TABLE I. DURING CHANNEL LENGTH IS 0.20μm

No.	Channel Length, L=0.20μm		
	Drain Voltage, V_D (V)	*Gate Bias (V)*	*Drain Current, I_D (μA)*
1.	0.1	0.3	751.44
2.	0.2	0.3	1193.58
3.	0.3	0.3	1793.72
4.	0.4	0.3	2620.30
5.	0.5	0.3	3730.34

From Table II, if drain voltage, V_D increasing, and gate bias is fixed at point of 0.3V, the drain current, I_D is increasing.

TABLE II. DURING CHANNEL LENGTH IS 0.30μm

No.	Channel Length, L=0.30μm		
	Drain Voltage, V_D (V)	*Gate Bias (V)*	*Drain Current, I_D (μA)*
1.	0.1	0.3	546.95
2.	0.2	0.3	638.89
3.	0.3	0.3	716.27
4.	0.4	0.3	793.03
5.	0.5	0.3	871.64

Based on Table II, if drain voltage, V_D increasing, and gate bias is fixed at point of 0.3V, the drain current, I_D is increasing moderately.

TABLE III. DURING CHANNEL LENGTH IS 0.40μm

No.	Channel Length, L=0.40μm		
	Drain Voltage, V_D (V)	*Gate Bias (V)*	*Drain Current, I_D (μA)*
1.	0.1	0.3	352.58
2.	0.2	0.3	388.12
3.	0.3	0.3	411.57
4.	0.4	0.3	431.69
5.	0.5	0.3	449.83

Meanwhile, based on Table III, if drain voltage, V_D increasing, and gate bias is fixed at point of 0.3V, the drain current, I_D is increasing moderately.

TABLE IV. DURING CHANNEL LENGTH IS 0.50μm

No.	Channel Length, L=0.50μm		
	Drain Voltage, V_D (V)	*Gate Bias (V)*	*Drain Current, I_D (μA)*
1.	0.1	0.3	321.61
2.	0.2	0.3	348.26
3.	0.3	0.3	364.80
4.	0.4	0.3	378.74
5.	0.5	0.3	390.59

Based on Table IV, if drain voltage, V_D increasing, and gate bias is fixed at point of 0.3V, the drain current, I_D is increasing slightly.

TABLE V. DURING CHANNEL LENGTH IS 0.20μm

No.	Channel Length, L=0.20μm		
	Drain Voltage, V_D (V)	*Gate Bias (V)*	*Drain Current, I_D (μA)*
1.	0.1	0.2	83.87
2.	0.2	0.2	134.19
3.	0.3	0.2	184.50
4.	0.4	0.2	285.14
5.	0.5	0.2	426.04

Based on Table V, if drain voltage, V_D increasing, and gate bias is fixed at point of 0.2V, the drain current, I_D is also increasing.

TABLE VI. DURING CHANNEL LENGTH IS 0.30μm

No.	Channel Length, L=0.30μm		
	Drain Voltage, V_D (V)	*Gate Bias (V)*	*Drain Current, I_D (μA)*
1.	0.1	0.2	160.72
2.	0.2	0.2	185.37
3.	0.3	0.2	206.43
4.	0.4	0.2	227.86
5.	0.5	0.2	250.02

Based on Table VI, if drain voltage, V_D increasing, and gate bias is fixed at point of 0.2V, the drain current, I_D is moderately increasing.

TABLE VII. DURING CHANNEL LENGTH IS 0.40μm

No.	Channel Length, L=0.40μm		
	Drain Voltage, V_D (V)	*Gate Bias (V)*	*Drain Current, I_D (μA)*
1.	0.1	0.2	97.20
2.	0.2	0.2	105.92
3.	0.3	0.2	111.73
4.	0.4	0.2	116.86
5.	0.5	0.2	121.63

Based on Table VII, if drain voltage, V_D increasing, and gate bias is fixed at point of 0.2V, the drain current, I_D is increasing slightly.

TABLE VIII. DURING CHANNEL LENGTH IS 0.50μm

No.	Channel Length, L=0.50μm		
	Drain Voltage, V_D (V)	*Gate Bias (V)*	*Drain Current, I_D (μA)*
1.	0.1	0.2	85.81
2.	0.2	0.2	92.21
3.	0.3	0.2	96.11
4.	0.4	0.2	99.43
5.	0.5	0.2	102.29

Based on Table VIII, if drain voltage, V_D increasing, and gate bias is fixed at point of 0.2V, the drain current, I_D is also slightly increasing.

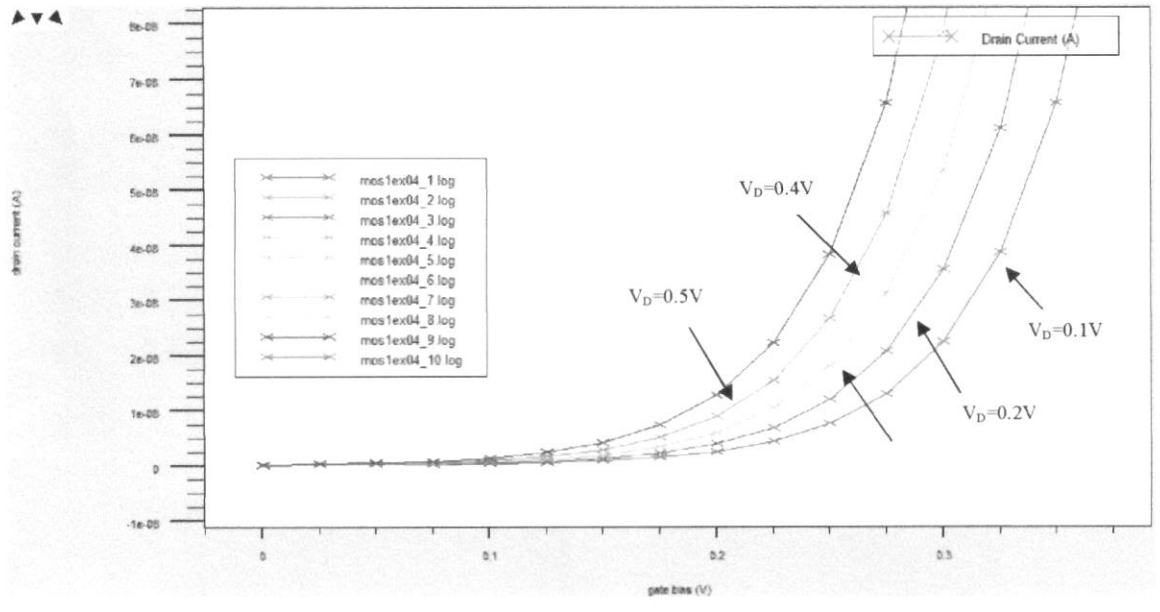

Figure 8: (a) I-V curve for DIBL extraction when channel length, L=0.20μm

From the results obtained, DIBL depends on how the drain current, I_D flows in the channel. The drain current, I_D is controlled by gate voltage, V_G and drain voltage, V_D. As the voltage drain, V_D is increasing, and the barrier height is decreasing while the drain current, I_D is increasing.

DIBL results in the increase in drain current, I_D at a given gate voltage, V_G. Therefore, the threshold voltage, V_{TH} decreasing as channel length, L decreasing. Likewise, as drain voltage, V_D increasing, drain current, I_D is also increasing and threshold voltage, V_{TH} is decreasing. These can be seen in the results of I-V curves as shown in the Figure 8 (a), (b), (c) and (d).

The values for I_D in the Table I, Table II and Table III, Table IV and Table V are based from the I-V curves in the Figure 8 (a), (b), (c) and (d). However, the values of I_D plotted in the curves are in ampere, A. To make the values easier to be compared, the values are converted into micro ampere, μA.

Figure 8(a) below shows the I-V curve for DIBL extraction when channel length, L is 0.20μm. As we can see from the graph, the I_D is increasing as the gate bias increasing. Same goes to Figure 8(b) and Figure 8(c) and Figure 8(d).

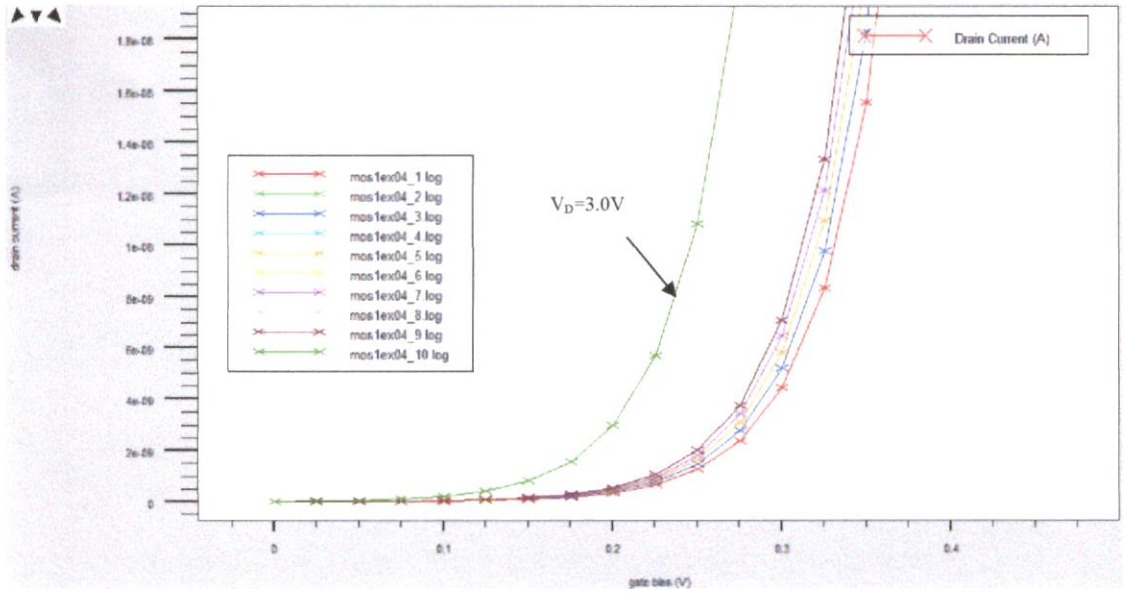

Figure 8: (b) I-V curve for DIBL extraction when channel length, L=0.30μm

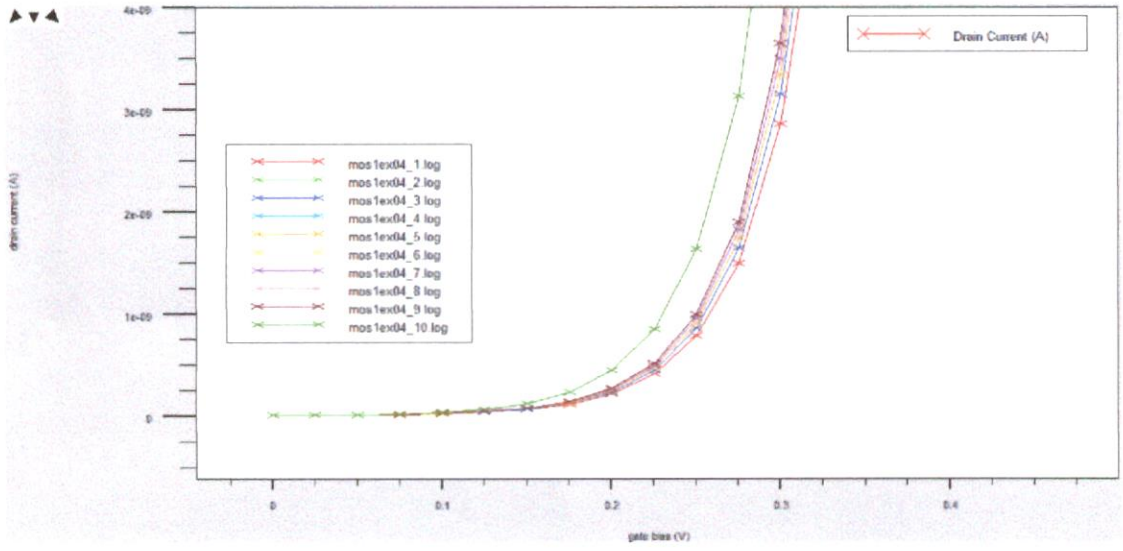

Figure 8: (c) I-V curve for DIBL extraction when channel length, L=0.40μm

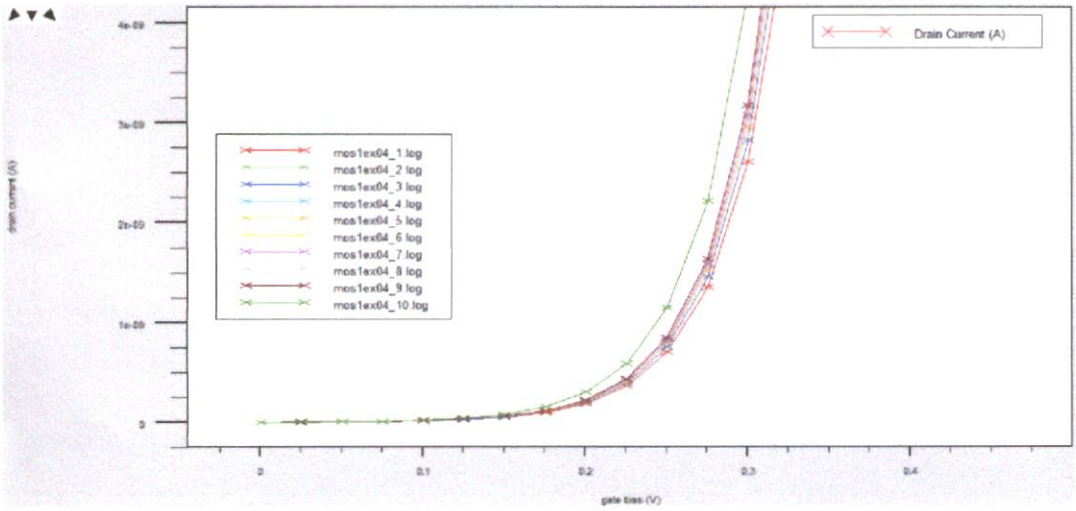

Figure 8: (d) I-V curve for DIBL extraction when channel length, L=0.50μm

From all the results obtained, the results then being summarized into Table IX and Table X to see the comparison between all the values.

TABLE IX. DURING GATE BIAS IS 0.3V

V_D (V)	I_D (μA)			
	L=0.20μm	*L=0.30μm*	*L=0.40μm*	*L=0.50μm*
0.1	751.44	546.95	352.58	321.61
0.2	1193.58	638.89	388.12	348.26
0.3	1793.72	716.27	411.57	364.80
0.4	2620.30	793.03	431.69	378.74
0.5	3730.34	871.64	449.83	390.59

From the Table IX, as channel length, L increasing, drain current, I_D is decreasing. Figure 9 below shows the I_D versus V_D graph when gate bias is 0.3V.

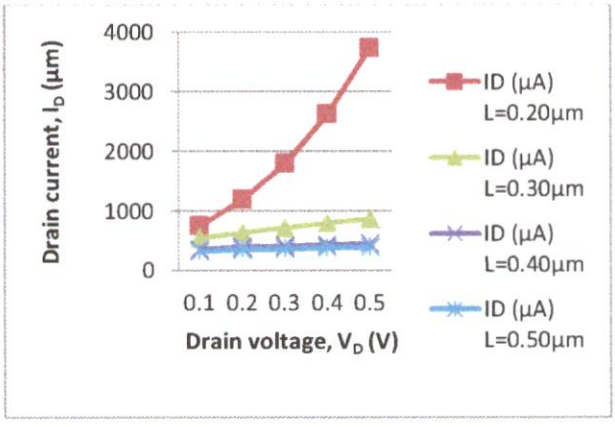

Figure 9: I_D versus V_D graph for gate bias=0.3V

TABLE X. DURING GATE BIAS IS 0.2V

V_D (V)	I_D (μA)			
	L=0.20μm	*L=0.30μm*	*L=0.40μm*	*L=0.50μm*
0.1	302.48	160.72	97.20	85.81
0.2	481.17	185.37	105.92	92.21
0.3	731.20	206.43	111.73	96.11
0.4	1085.51	227.86	116.86	99.43
0.5	1372.32	250.02	121.63	102.29

Meanwhile, from the Table X, as channel length, L increasing, drain current, I_D is decreasing. Figure 10 below shows the I_D versus V_D graph when gate bias is 0.2V. However, as drain voltage increased, the drain current is also increased.

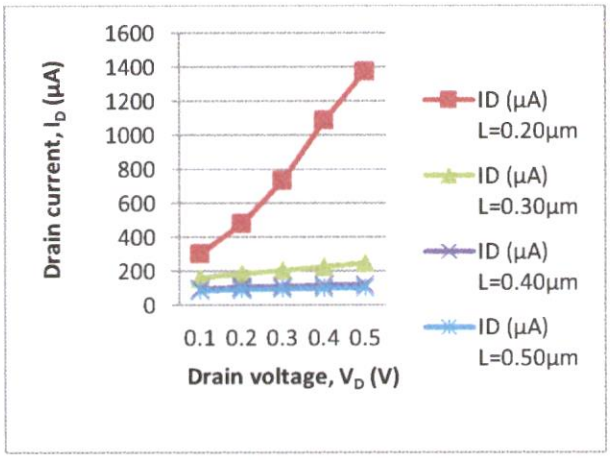

Figure 10: I_D versus V_D graph for gate bias=0.2V

Also, from the simulation done, the results for DIBL shows that as the channel length is decreasing, the more DIBL occurs. This can be shown in the Table XI below.

TABLE XI. DIBL

No.	*Channel Length, L(μm)*	*DIBL(mV/V)*
1.	0.20	11.9556
2.	0.30	10.9188
3.	0.40	10.7004
4.	0.50	10.6628

Figure 11 shows the graph of DIBL versus channel length, L. From that graph, it is true that DIBL increased as the channel length, L decreased.

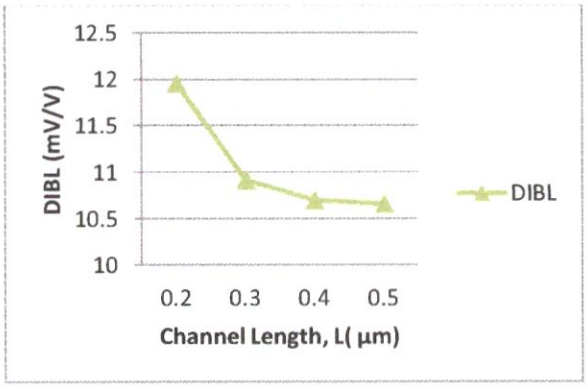

Figure 11: DIBL versus Channel Length, L

VI. CONCLUSION

The purpose for this project is to study about the DIBL in MOSFET and to implement and simulate MOSFET structure that has DIBL using SILVACO software. The MOSFET used is NMOS. As the conclusion, this paper achieved the objectives of the project where the objective of this project is to study and simulate DIBL in MOSFET and to compare the MOSFET structures when the channel length, L is varies and to compare I-V curves when the value of drain voltage, V_D are varies. DIBL depends on how the drain current, I_D flows in the channel. As the drain voltage, V_D is increasing, the potential barrier in the channel decreasing and this leads to DIBL. As the voltage drain, V_D is increasing, and the barrier height is decreasing while the drain current, I_D is increasing. For further study, the future recommendation is to reduce or minimize the DIBL. There are few ways to reduce DIBL such as we can reduce the capacitance junction, Xj, increase substrate doping concentration and reduce oxide thickness use in the project.

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REFERENCES

[1] E.F. Schubert, "MOSFET-Basics", Rensselaer Polytechnic Institute, 2003. Available: http://www.ecse.rpi.edu/~schubert/Course-ECSE-6290%20SDM-2/1%20MOSFET-1%20Basics.pdf

[2] Fabio D'Agostino and Daniele Quercia, "Short Channel Effects in MOSFETs", December 11th, 2000.

[3] Hashimah Hashim,Shafinaz Sobihana Shariffudin, Puteri Sarah Mohamad Saad 'Study the Effect of Drain Induced Barrier Lowering (DIBL) in CMOS Device by Using SILVACO TCAD', Universiti Teknologi Mara, June 2007.

[4] M.A. Karim Sriramkumar V., Yogesh S.C., Darsen Lu, Ali Niknejad and Chenming Hu,"Drain Induced Barrier Lowering (DIBL) Effect on the Intrinsic Capacitances of Nano-Scale MOSFETs", University of California at Berkeley, 2011.

[5] Dr. Lynn Fuller,"2D Process Modeling with Silvaco ATHENA", Microelectronic Engineering Rochester Institute of Technology, 11-15-2010 silvaco.ppt. Available: http://people.rit.edu/lffeee/SILVACO.pdf

[6] S . M. Sze, "Physics of Semiconducror Devices", New York, Wiley, 1981.

[7] Salehuddin Fauziyah, Obrahim Ahmad, Fazrena Azlee Hamid, Azami Zaharim, "Analyze and Optimize the Silicide Thickness in 45nm CMOS Technology using Taguchi Method", University Tenaga Nasional, 2010.

[8] M. Jamal Deen, and Z. X. Yan, "DIBL in Short-Channel NMOS Devices at 77 K", IEEE Trans. Electron Devices, vol. 39, no. 4, April 1992.

[9] Michael J. Van der Tol and Savvas G. Chamberlain, Fellow, IEEE,"Drain-Induced Barrier Lowering in Buried-Channel MOSFET's", Department of Electrical Engineering,University of Waterloo, Waterloo, Ont. Canada, April 1993.

[10] Tang, D.D.-L., Hackbarth, E., Chen, T.-C., "On the very-high-current degradations on Si n-p-n transistors", IBM T.J. Watson Res. Center, Yorktown Heights, NY, USA, Electron Devices, IEEE Transactions on (Volume:37 , Issue: 7).