

Study on the Effect of Etching Process of NMOS Structure Using SILVACO TCAD Tools

Mohd Shahrir Abd Rahim

Faculty of Electrical Engineering
Universiti Teknologi MARA
40450 Shah Alam, Selangor, Malaysia
mdshah8@yahoo.com

Abstract – The effect due to the etching process of NMOS structure using Silvaco TCAD tools was investigated using different etching methods by varying the etch rate and divergence rate. The etching methods are isotropic wet etching method and isotropic RIE etching method where the length of polysilicon gate and threshold voltage were decreased by increasing the etch rate. The chemical RIE etching method provided highly selectivity and directionality gives various divergence rates. The directional RIE etching method gave similarities in term of etch profile, junction depth and threshold voltage characteristic compared to the reference geometrical etching method for any etch rate and divergence rate.

Keywords: Chemical RIE etching; Directional RIE etching; Divergence rate; Etch rate; Geometrical etching; Isotropic RIE etching; NMOS; Silvaco TCAD; Wet etching

1.0 INTRODUCTION

1.1 Overview

For more than 30 years, MOS device technologies have been improving at a dramatic rate [4]. The NMOS has continually been scaled down in size, typical NMOS channel lengths were once several micrometers, but nowadays the channel length of an NMOS is about a 35 nanometer. The implementation of a smaller NMOS is related to the performance of the device. There are two main reasons. Firstly, smaller NMOSs allow more current to flow. Secondly, smaller NMOSs have smaller gates, and thus lower gate capacitance. These two factors contribute to a quicker switching duration which leads to producing a faster device in terms of data processing. Smaller NMOSs can obviously be packed more densely, resulting in either smaller chips or chips with more computing power in the same area [2]. In order to fabricate the NMOS in nanometer size, it requires a very precise fabrication technology. Although there are many parameters that have an influence on the threshold voltage, the investigation

in this research is scaled down to concentrate on the effect of etching process to the device performance.

Integrated circuit (IC) and their elements must be released with high precision [3]. The basic functional element on an integrated circuit is the transistor; most commonly silicon Metal Oxide Semiconductor Field-Effect Transistor (MOSFET). The three MOSFET's terminals are called Gate (G), Source (S) and Drain (D) as shown in the Fig.1. MOSFET constitutes of two different types which are P-channel and N-channel types. The fabrication process of an NMOS requires a very high accuracy in every step taken especially in the lithography step.

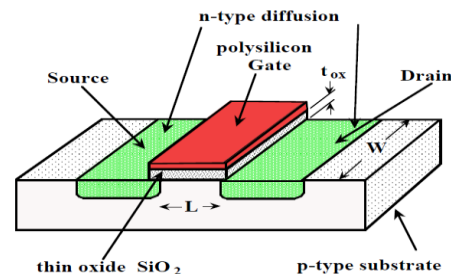


Fig.1: NMOS Structure.

Photolithography is basically a means to protect desired areas of the wafer while the device is fabricated. The exposed areas are etched away as they were not protected. The protective material is called a photoresist. There are positive and negative photoresist. When the photoresist is removed after completing etching process, the polysilicon is formed to define the gate region of an NMOS. The method by which material is removed from the wafers varied depending on the geometry feature size, the amount of material to be removed, the thickness of the material, and the level of uniformity also the shape required.

The etching process in nanometer size affects the performance of the device. By using Silvaco Technology Computer Aided Design (TCAD) software, the etching process can be selected by using two different methods; wet etching and dry

etching method. The geometrical etch is the default method [1].

Two important figures of merit for any etching process are selectivity and directionality [3]. Selectivity is the degree to which the etchant can differentiate between the masking layer and the layer to be etched. Whereas, directionality associates with the etch profile under the photoresist. The etch profile shape depends on the method of etching. In a shape of an isotropic, the etchant attacks the material in all directions at the same rate, creating a semicircular profile under the PR as shown in Fig.3. On the other hand, for an anisotropic shape, the dissolution rate depends on specific directions, and one can obtain straight sidewalls or other noncircular profiles as shown in Fig.4.

1.2 Objective of Research

The main objective of the study is to investigate the effect of utilizing different etching process using Silvaco Technology Computer Aided Design (TCAD) software on the NMOS structure. By varying the rate of each etching methods, the characteristics of the NMOS obtained were different. Therefore, the summary of objectives and aims of this project are:

- To apply the etching rate and divergence rate by using different etching methods.
- To achieve the optimum parameter of etch rate and divergence rate as a step in obtaining the best performance of an NMOS structure.

1.3 Scope of Work

The scope of work for this research is to study the effect of the etching process with different methods on an NMOS structure. In order to achieve the objective of this project, a simulation of a full NMOS structure using Athena process simulation and Atlas device simulation of the Silvaco TCAD software was performed. In the etching process of the polysilicon in NMOS structure, the etching machines have to be considered using optimum rate of etching. Only an isotropic etch profile is available for the wet etching method. In contrast, the dry etching method which is a Reaction Ion Etching (RIE) has three types that can be chosen. The types are isotropic, directionality and chemical. Since the focus of this research is to study the effect of etching at polysilicon layer, the rate of etching machine must be varied to find the optimum etching rate in order to obtain the optimized result. Hence, the optimum

etching rates are achieved from the I_D-V_{GS} characteristic curve and were analyzed.

1.4 Literature Review

1.4.1 Overview of NMOS

The basic structure of an n-channel enhancement type MOSFET (N-Channel MOS or NMOS) contains a source, gate and drain contact as in Fig.1. The source and drain contacts are connected to the n-type source and drain regions respectively. These regions are two heavily doped n+ regions with shallow donors so that they contain a large number of mobile electrons. Between these two regions exists a narrow region called the channel. The physical distance between the source and drain is the channel length; L which is also called gate length of the NMOS. The channel length of a NMOS is defined as the distance from the edge of the source region to the edge of the drain region in the device. The channel length is one of the key parameter that characterizes the device. The substrate is a moderately doped p-type silicon substrate and doped with acceptors. P-N junctions exist between the source and the substrate as well as between the drain and the substrate [2].

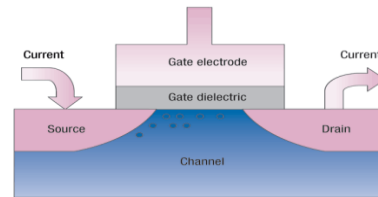


Fig.2: Operation of NMOS.

When the gate is biased positively, it will generate positive charges (N-channel) at the surface of the P region, just under the oxide, by depleting this region of holes as shown in Fig.2. This channel extends between the source and the drain. Current is conducted through it but only when the gate potential is highly enough to attract electrons from the source into the channel. Therefore, electrons shall move from the source to the drain creating an electric current. As the gate voltage is increased, the drain current increases while the output voltage decreases. On the contrary, the drain voltage decreases despite the increase in drain current causing the depletion region between the drain and the substrate decreased. When the gate voltage is higher than the threshold voltage, the silicon-oxide surface will accumulate enough electrons to form a channel and allow electrons from source and drain to flow across it [5].

When the gate is not biased, no current can go through from source to drain regardless the effort in biasing the source-drain. The source is named in such a manner because it plays the role as a source of charge carriers (electrons for N-channel, holes for P-channel) that flow through the channel. Similarly, the drain is where the charge carriers leave the channel. When a voltage applied across the insulating gate oxide, it causes carriers to accumulate below the gate oxide. This creates a conducting channel that controls current to flow from source to drain.

1.4.2 Etching Method

The etching process is used in order to etch away undesired parts such as polysilicon and silicon dioxide (SiO_2) of a material. Etching processes are necessary and is one of the critical parts in integrated-circuit processing technology. Etching refers to the removal of material from the surface of a wafer using either a chemical or mechanical process, or even a combination of both. Etching processes are needed to pattern a deposited layer and to form contact opening in dielectric layers. This deposited layer shall connect the metal layer to the substrate through the dielectric layers. The methods by which material is removed from the wafers vary depending on the geometry feature size, the amount of material to be removed, the thickness of the material, and the level of uniformity and anisotropy required [4].

The methods of etching using Silvaco TCAD tools are geometrical, wet etching and reactive ion etching (RIE). Wet etching uses chemical reactions between liquid reactants and the wafer surface to remove material. In wet etching, the liquid reactant reacts with the material at the surface of the wafer to form a product that is soluble in the liquid. The solution's temperature, molar strength of the reactants, and the length of time where the wafer is immersed in the solution affect the amount and uniformity of the material that was removed.

Wet etching may be used for isotropic material removal depending on the etchant and the substrate film. Advantages of wet etching are high selectivity between the material to be etched and other materials on the wafer, and minimal substrate damage. However, wet etching does pose problems for uniformity, anisotropy and process control. Reactive Ion Etching (RIE) is an etching method performed in a low-pressure gaseous discharge; therefore, the chemical reaction responsible for the etching action occurs in the gas phase with the assistance of the plasma. These etch processes provide better etch rate uniformity and control as

well as very pronounced anisotropic etching. The high etch rate selectivity of wet etching is good compared to RIE etch method, but RIE is well-compensated and better uniformity.

1.4.3 Etch Profiles

In etching, there are different kinds of shape. The shape of the feature that is etched is called the etch profile. The etch profile separates into two types; isotropic and anisotropic shapes. Normally, wet etches are typically isotropic while dry etches are anisotropic. In most cases, the desired etch profile is square shape. To obtain this perfect profile, etch and passivation have to be carefully balanced and if need to be readjusted as the aspect ratio of the structure increase. Excessive sidewall passivation leads to tapered profiles that are desired for shallow trench isolation etch. The lack of sidewall passivation and excessive spontaneous chemical etching results in creating ion deflection. Hence, this leads to an existence of an undercutting. Ion deflection in very narrow spaces can lead to bowing. At the interfaces of layers such as the interface between the gate oxide and the poly-Si layer, notching has to be avoided [6].

Isotropic etch profile has an equal area of etching polysilicon in all directions; vertically and laterally. This is so because the lateral etches rate is about the same as vertical etches rate. Wet etch usually give isotropic etch profile shape. This is because the isotropic etch rate does not depend on the orientation of the mask edge. It is very difficult to define small features with an isotropic etch which may cause etch resolution becomes fairly poor. In accordance to that, dry etching is required to associate very small features. However, there are some dry etches also give isotropic profiles.

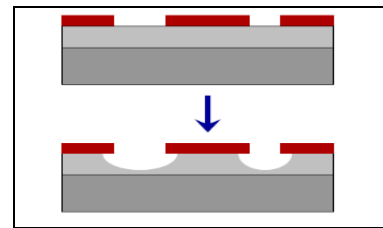


Fig. 3: Isotropic etch profile.

On the other hand, anisotropic etch profile is an etch rate dependent on orientation to the crystalline planes. Using an etch rate machine, etch rate can be choose to transfer lithographic patterns for smaller features to be etch in the preferred direction only. The lateral etch rate can be much larger or smaller than vertical etch rate, depending on

orientation of mask edge to crystalline axes. It is totally dependent on the orientation of mask edge and the details of the mask pattern in order to determine the final etched shape. The anisotropic etch profile only occurs in a dry etch method.

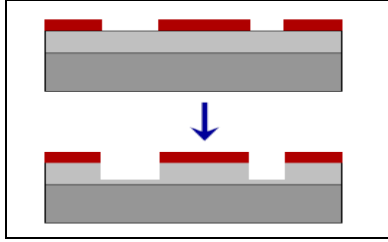


Fig. 4: Anisotropic etch profile.

2.0 METHODOLOGY

Athena and Atlas module of Silvaco software are the tools used in simulating the fabrication process and extracting simulation of electrical performance of the NMOS devices respectively as shown in Fig.5. The fabrication flow of NMOS structure was performed in the 'deckbuild'. Once the device has been created, the electrical property such as the I_D - V_{GS} curve which defines threshold voltage can be extracted in Atlas.

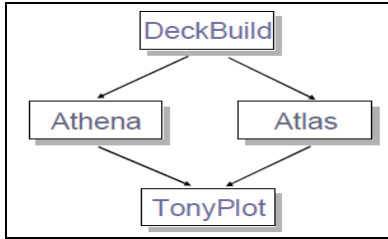


Fig.5: Silvaco Athena and Atlas.

The flow to fabricate of an NMOS structure used in Athena for all the five etching methods which are wet etching method, geometrical, directional RIE, isotropic RIE and chemical RIE was similar except during the etching process. This means that the rest of the steps in fabricating the NMOS structure such as diffusion, ion implantation and annealing process are still the same for all five etching methods. The methods of etching can be selected at the 'Athena Etch menu'. The parameters rate for each method also can be varied in the menu. The etch profile parameters that were used in this research is as shown in Fig.6.

In this paper, the etching for polysilicon of NMOS fabrication processes by using geometrical etching, wet etching and reactive ion etching (RIE)

method was studied. The photoresist mask was pattern for 0.50 μm length of polysilicon and this was used for all the three etching methods. There were three main NMOS properties that have been observed. The properties are the etch profile structure, junction depth and threshold voltage. In each property, two different parameters were varied which are the etch rate and divergence rate to study the effect of those parameters on the NMOS properties.

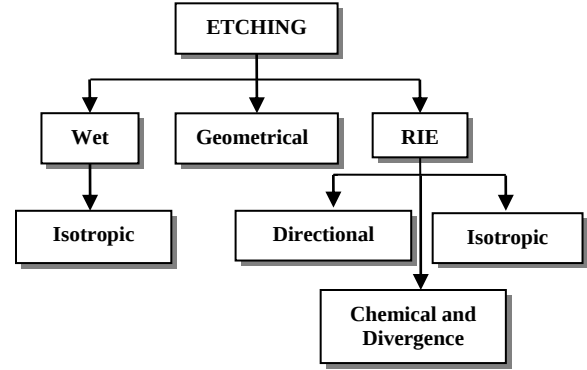


Fig.6: Etch Profile Parameter for Silvaco.

The study regarding on the effect of etch rate ($\text{\AA}/\text{Sec}$) for different etching methods constitute of four etching methods which are wet etching, isotropic RIE etching, directional RIE etching and chemical RIE etching has been done by varying the etch rate. Three etch rate values were used which are 33 $\text{\AA}/\text{Sec}$, 36 $\text{\AA}/\text{Sec}$ and 39 $\text{\AA}/\text{Sec}$. As this was performed, the divergence rate was fixed as constant at 0.01 $\text{\AA}/\text{Sec}$. The effect of using these three different values of etch rate on the etch profile, junction depth and threshold voltage has been investigated.

The study regarding on the effect of divergence rate ($\text{\AA}/\text{Sec}$) for different etching methods constitute of three etching methods which are isotropic RIE etching, directional RIE etching and chemical RIE etching has been studied by varying the divergence rate. Same as etch rate, divergence rate uses three values which are 5 $\text{\AA}/\text{sec}$, 10 $\text{\AA}/\text{sec}$ and 15 $\text{\AA}/\text{sec}$. As this was performed, the etch rate was fixed as constant at 33 $\text{\AA}/\text{Sec}$. The effect of using these three different values of divergence rate on the etch profile, junction depth and threshold voltage has been investigated.

Three etch rate parameters were chosen based on the appropriateness for all methods. The result of each method was compared to geometrical etching which acts as a benchmark for the whole

research. Using geometrical etching method, the undesired location of polysilicon is etched away directly following the pattern of the photoresist masking. It results in achieving the desired NMOS structure.

3.0 RESULTS AND DISCUSSION

This chapter is divided into three sections. First section describes the effects on etch profiles by using different etching method. The second section discusses the effect on junction depth. The last section investigates the effect on threshold voltage by using different etching method.

3.1 EFFECT ON THE ETCH PROFILE BY USING DIFFERENT ETCHING METHODS

In this research, geometrical etching was set as a reference etching method in the Silvaco. As a reference, the geometrical etching gave a perfect result where the length of etched polysilicon was similar to the length of photoresist masking. It was found that through geometrical etching, the etched polysilicon length was $0.50\ \mu\text{m}$ as shown in Fig.7.

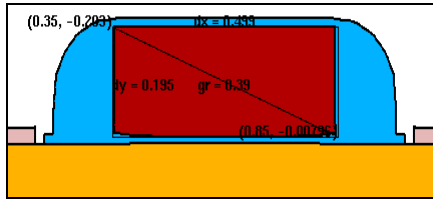


Fig.7: Geometrical Etching.

The study of the etching process effect were carried out by using four etching methods which are wet etching method, isotropic RIE etching method, directional RIE etching method and chemical RIE etching method.

3.1.1 Effect of etch rate on the etch profile at different etching methods. (divergence rate = $0.01\text{\AA}/\text{Sec}$)

From the Silvaco simulation result, the wet etching gave an isotropic etch profile as shown in fig. 8. The results show that the polysilicon was etched away at all directions. However, the profiles suggested that the wet etching does not depend on the orientation of the photoresist mask pattern. The profile shows that the polysilicon was etched away much deeper laterally at the top of polysilicon than at the bottom. The etch profiles for different etch rates also have been studied as showed in fig.8 (a), fig.8

(b) and fig.8 (c). The results show that by increasing the etch rate, the length and area size of polysilicon were decreased. As a result, higher etch rate gives smaller surface segments of the polysilicon.

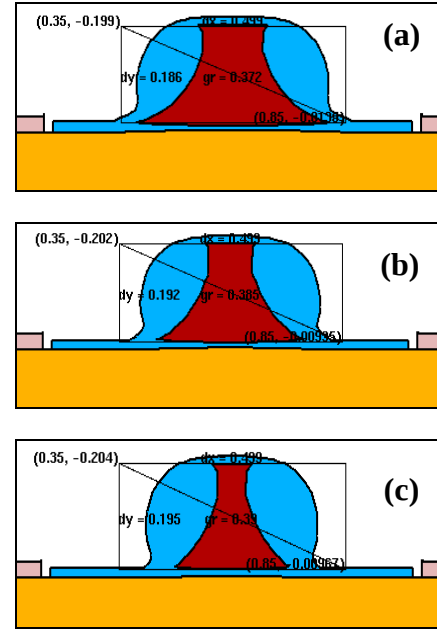


Fig.8: Isotropic wet etching profiles at etch rates of (a) $33\text{\AA}/\text{sec}$, (b) $36\text{\AA}/\text{sec}$ and (c) $39\text{\AA}/\text{sec}$.

The etching profiles using isotropic RIE etching method was shown as in fig. 9(a), fig. 9 (b) and fig. 9 (c).

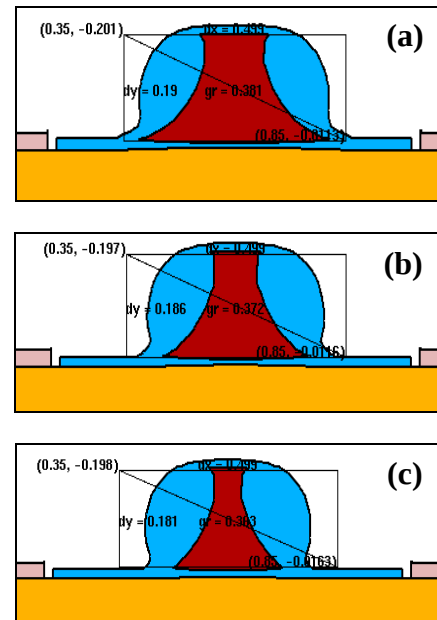


Fig.9: Isotropic RIE etching profiles at etch rates of (a) $33\text{\AA}/\text{sec}$, (b) $36\text{\AA}/\text{sec}$ and (c) $39\text{\AA}/\text{sec}$.

In the isotropic RIE etching method, it was found that the etched polysilicon shape was similar as obtained by isotropic wet etching. The profiles for different etch rates also show similar pattern with the profiles of isotropic wet etching where the length and area size of etched polysilicon have been decreased due to the increasing of etch rates.

For the NMOS structure that was used in this research, the etch rate for isotropic wet etching and isotropic RIE were in the range between 32 Å/sec and 41 Å/sec. The isotropic wet etching method and isotropic RIE etching method cannot tolerate with other etch rate. It is because etch rate other than these two values will either etched polysilicon entirely or obtaining an undesired structure. It means that the isotropic wet etching method and isotropic RIE etching method were suitable to be used at large geometrical when sidewall is non-critical.

By choosing the directional RIE etching method, the specific location can be etched. As shown in fig.10 (a), fig.10 (b) and fig.10 (c), the polysilicon shaped by using directional RIE etching was almost similar to the shaped of etching by using geometrical etching method. The polysilicon was vertically cut with no laterally etched.

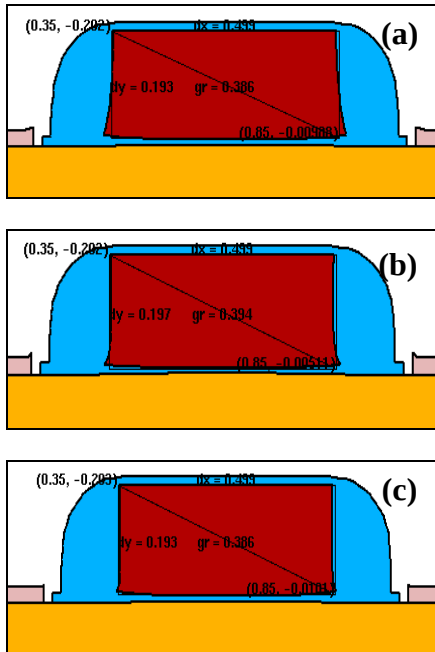


Fig.10: Directional RIE etching profiles at etch rates of (a) 33Å/sec, (b) 36Å/sec and (c) 39Å/sec.

By increasing the etch rate, the both sides of polysilicon pattern becomes more flat. The results have shown that the directionality have been

achieved by increasing the etch rate. Also, the directional RIE etching method was an orientation dependent, capable of controlling etch rate and reduces etch damage to the polysilicon. The polysilicon etched by using the directional RIE etching method gives an anisotropic etch profile. The anisotropic etch profile gives a straight cut vertically to the polysilicon.

In order to etch polysilicon by using chemical RIE etching method, it was depending on the divergence of ion that collided to polysilicon. The simulation result showed in fig.11 (a), fig 11(b) and fig 11(c) for etch rate set at 33 Å/sec were almost similar to the polysilicon patterned by using geometrical etching method. By observation, there was no different in polysilicon structure. The etch rate controls the movement of ions collided to the surfaced of polysilicon. Theoretically, the increment of etch rate gives enhancement to the velocity of ions movement. Therefore, the speed of etching process due to the increase in the chemical etch rate become faster.

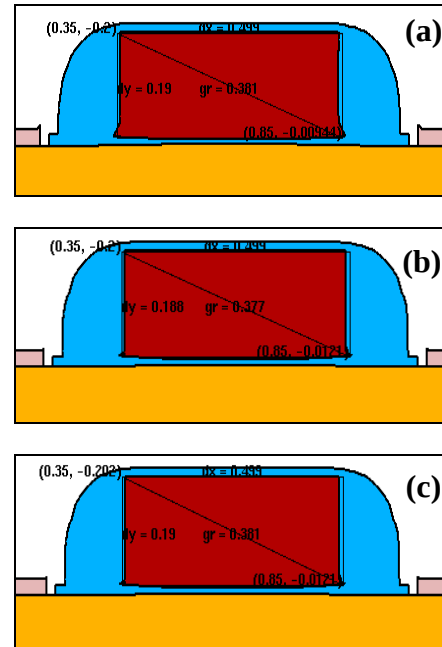


Fig.11: Chemical RIE etching profiles at etch rates of (a) 33Å/sec, (b) 36Å/sec, and (c) 39Å/sec.

3.1.2 Effect of divergence rate on the etch profile at different etching methods. (etch rate = 33Å/Sec)

From the Silvaco simulation result, the isotropic RIE etching method gave an isotropic etches profile as shown in fig.12. The results show

that the polysilicon was etched away at all directions. However, the profiles suggested that the isotropic RIE etching method is independent on the orientation of the photoresist mask pattern. The profile shows that the polysilicon was etched away much deeper laterally at the top of polysilicon than at the bottom. The etch profiles at different divergence also have been studied as showed in fig.12 (a), fig.12 (b) and fig.12 (c). By observations, the results show that by increasing the divergence, the length and area size of polysilicon were unchanged. As a result, the divergence does not affect the etch profile of the polysilicon.

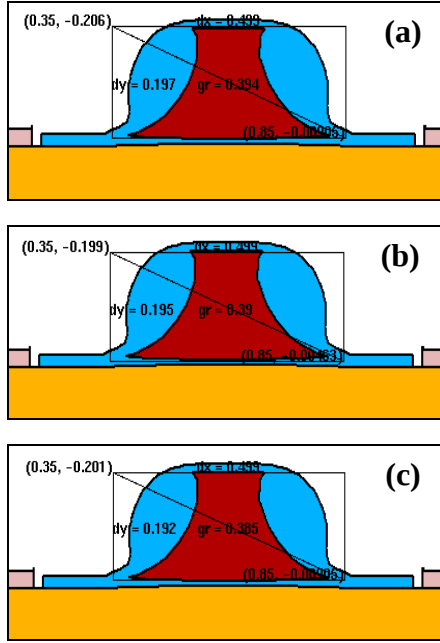


Fig.12: Isotropic RIE etching profiles at etch rates of 33 Å/sec, with divergence of (a) 5 Å/sec, (b) 10 Å/sec and (c) 15 Å/sec.

By choosing the directional RIE etching method, the specific location can be etched. As shown in fig.13 (a), fig.13 (b) and fig.13 (c), the polysilicon shape was almost similar to the shape of etching by using geometrical etching method. The polysilicon was vertically cut with no laterally etched. There was an unchanged of polysilicon pattern by increasing the divergence. It shows that the directional RIE etching method was an orientation dependent, controllable of only etch rate and reduces etch damage to the polysilicon.

The polysilicon etched by using the directional RIE etching method gives an anisotropic etch profile. The anisotropic etch profile give straight cut vertically to the polysilicon.

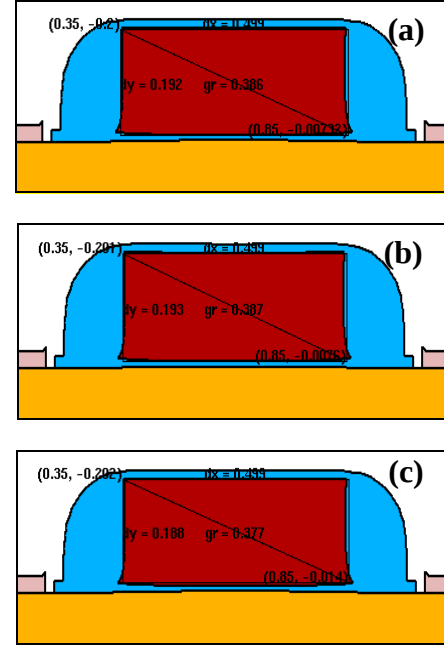


Fig.13: Directional RIE etching profiles at etch rates of 33 Å/sec, with divergence of (a) 5 Å/sec, (b) 10 Å/sec and (c) 15 Å/sec.

In the chemical RIE etching, divergences of the ions coming down to the wafer were varied at three rates which are 5 Å/sec, 10 Å/sec and 15 Å/sec. At the same time, the chemical divergence was fixed at 33 Å/sec. The results for a setting of 33 Å/sec were showed in fig.14 (a), fig.14 (b) and fig.14(c).

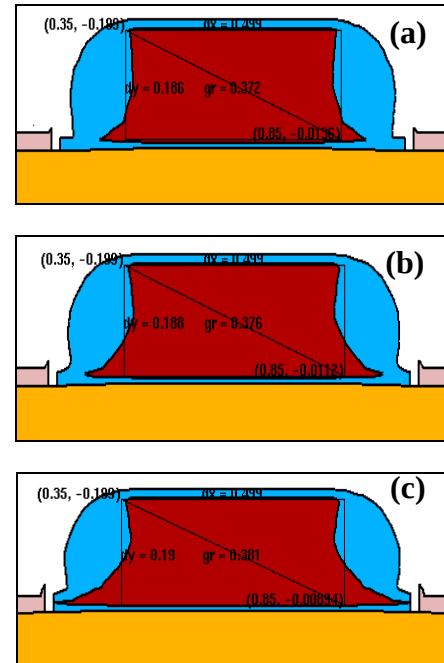


Fig.14: Chemical RIE etching profiles at etch rates of 33 Å/sec, with divergence of (a) 5 Å/sec, (b) 10 Å/sec and (c) 15 Å/sec.

When the divergences rate decreased, the polysilicon was etched vertically. As divergence increased the profile of etching by using the chemical RIE etching methods was potentially more isotropic. Fig.14 shows that the length and area size of etched polysilicon were increased by the increment of the divergences. It was found that the divergence rate controls the angle of etching. The increasing of divergence rate causes the anisotropic etch profile to switch and become an isotropic etches profile.

3.2 EFFECT ON THE JUNCTION DEPTH BY USING DIFFERENT ETCHING METHODS

The junction depth of the NMOS structure device was studied in term of the effect by using different etching methods. Lower junction depths result an increment of resistance in the substrate. When the resistance of substrate was high, it gave performance degradation to the device. In order to study the effect of the etching method to the junction depth, the etch rate and divergence for all methods have to be manipulated respectively. Table 1 shows the values of junction depth for differences etch rate while table 2 described the values of junction depth for a different divergence in the etching method that was obtained from the simulation. The junction depth of geometrical etching method was shown in fig.13.

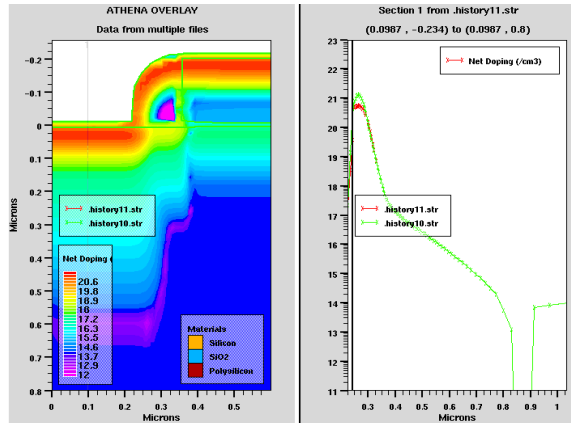


Fig.13: Junction depth for geometrical etching.

An equal concentration of n-type and p-type in the substrate defines the junction depth of the device. The green line represents net doping before the annealing process while the red line represents the net doping after the annealing process. This graph gives information about the doping profile and junction depth. The junction depth is the intersection between two doping line overlay before and after annealing process. It shows that the junction depth for geometrical etching was 0.595944 μm

3.2.1 Effect of etch rate on the junction depth by different etching methods. (divergence rate = 0.01 $\text{\AA}/\text{Sec}$)

The isotropic wet etching method and isotropic RIE etching method have similar values of junction depth. From the observation of using all etching methods, the junction depth has increased rapidly for an etch rate of 33 $\text{\AA}/\text{Sec}$ until the etch rate arrived at 36 $\text{\AA}/\text{Sec}$. Then, the etch rate increased gradually as shown in the fig.14.

Table 1: Effect of etch rate on the junction depth by different etching methods. (divergence rate = 0.01 $\text{\AA}/\text{Sec}$)

Etch Rate ($\text{\AA}/\text{Sec}$)		Junction Depth (μm)		
		33	36	39
Etching Method	Wet Isotropic	0.589339	0.595949	0.595957
	RIE Isotropic	0.589339	0.595949	0.595957
	RIE Directional	0.589456	0.595944	0.595943
	RIE Chemical	0.589460	0.595945	0.595945

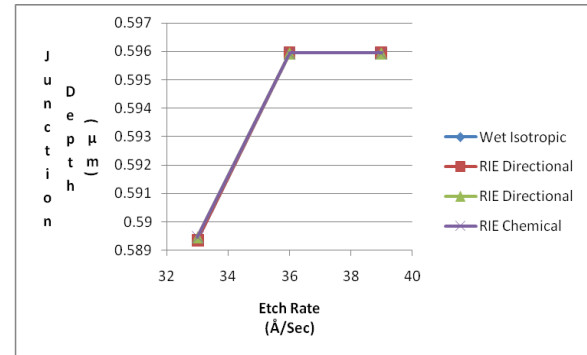


Fig.14: Effect of etch rate on the junction depth at different etching methods. (divergence rate = 0.01 $\text{\AA}/\text{Sec}$)

Although the pattern of etch profile has affected the length of polysilicon (critical dimension) of the device, it has not given much affect to the junction depth of the device. This was obtained after making comparison with the differences of methods that were used. There were no differences in junction depth for etch method.

3.2.2 Effect of divergence rate on the junction depth by different etching methods. (etch rate = 33Å/Sec)

Table 2 shows the values of junction depth with the variation of divergence rate for three etching method which are isotropic RIE etching method, directional RIE etching method and chemical RIE etching method that were obtained from the simulation. The wet etching was unrelated to the divergence. For the isotropic RIE etching method and directional RIE etching method, the junction depth does not effect to the changing of divergence rate.

Table 2: Effect of divergence rate on the junction depth for different etching methods. (etch rate = 33Å/Sec)

		Junction Depth (μm)		
Divergence ($\text{\AA}/\text{Sec}$)		5	10	15
Etching Method	RIE Isotropic	0.589339	0.589339	0.589339
	RIE Directional	0.589456	0.589456	0.589456
	RIE Chemical	0.58946	0.589271	0.586629

The value of junction depth unchanged for any divergence rate using isotropic RIE etching method and directional RIE etching method. In contrast, the chemical RIE etching methods have influenced the junction depth due to the changing of divergence. The junction depth was constant from a setting between 5° until 10° angle and drops rapidly by increasing the divergence angle.

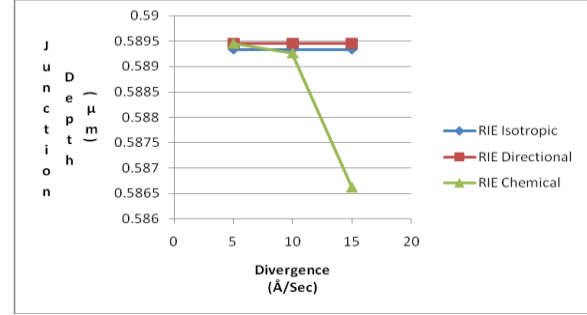


Fig.15: Effect of divergence rate on the junction depth at different etching methods. (etch rate = 33Å/Sec)

3.3 EFFECT ON THE THRESHOLD VOLTAGE BY USING DIFFERENT ETCHING METHOD

The electrical behaviours of the NMOS device are studied by making comparison on the threshold voltage for the different of etching methods. Table 3 shows the values of threshold voltage for different etch rate while table 4 described the threshold voltage for a different divergence in the etching method that was obtained from the simulation. The threshold voltage of geometrical etching method was 0.203864 V.

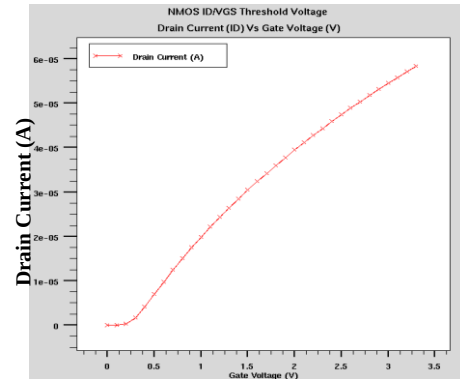


Fig.16: The graph of NMOS I_D - V_{GS} threshold voltage by geometrical etching method.

Fig.16 shows the graph of I_D - V_{GS} curve which defines the threshold voltage. The threshold voltage of geometrical etching method was 0.203864 V. The graph shown in the fig.17 was NMOS I_D - V_{DS} threshold voltage. There were three settings of gate voltages which were 1.1 V, 2.2V and 3.3 V.

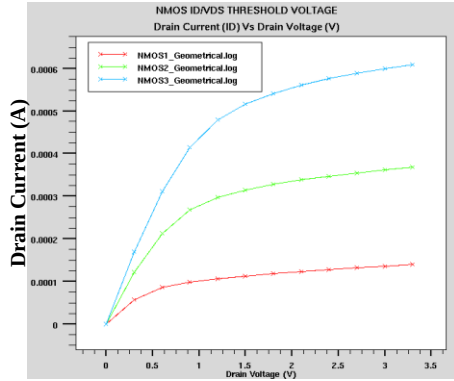


Fig.17: The graph of NMOS I_D - V_{GS} threshold voltage by geometrical etching method.

3.3.1 Effect of etch rate on the threshold voltage by different etching methods (divergence rate = $0.01 \text{ \AA/Sec}$)

Table 3 shows the tabulated result of threshold voltage by varying the etch rate for isotropic wet etching method, isotropic RIE etching method, Directional RIE etching method and chemical RIE etching method. By using isotropic wet etching, the threshold voltages were increased for the decrement of etch rate. It was similar characteristic of threshold voltage by using isotropic RIE etching method.

Table 3: Effect of etch rate on the threshold voltage by different etching methods. (divergence rate = $0.01 \text{ \AA/Sec}$)

		Threshold Voltage (V)		
Etch Rate ($\text{\AA/Sec}$)		33	36	39
Etching Method	Wet Isotropic	0.139827	0.112917	0.069653
	RIE Isotropic	0.139830	0.112917	0.069653
	RIE Directional	0.197792	0.201778	0.205435
	RIE Chemical	0.196768	0.199560	0.199560

The threshold voltage was decreased constantly as the increased of etch rate. In contrast, the threshold voltage of directional RIE etching method and chemical RIE etching method was increased gradually. The different values on the threshold voltages by using different etching methods were shown in the fig.18. The minimal changed of threshold voltage had occurred in the directional RIE etching method and chemical RIE etching method as etch rate varied.

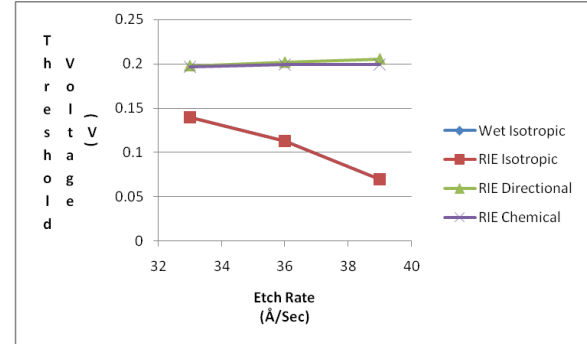


Fig.18: Effect of etch rate on the threshold voltage by different etching methods. (divergence rate = $0.01 \text{ \AA/Sec}$)

3.3.2 Effect of divergence rate on the threshold voltage by different etching methods. (etch rate = $33 \text{ \AA/Sec}$)

Table 4 shows the values of threshold voltage with the various divergence rates for three etching methods which are isotropic RIE etching method, directional RIE etching method and chemical RIE etching method that was obtained from the simulation.

The wet etching was unrelated to the divergence. For the isotropic RIE etching method and directional RIE etching method, the threshold voltage does not effect to the changing of divergence. The value of threshold voltage unchanged for any divergence rate. However, the threshold voltage of directional RIE etching method was nearly to threshold voltage of geometrical etching compared to isotropic RIE etching.

In contrast, the chemical RIE etching method has affected the threshold voltage for several of divergence rate. The threshold voltage was increased gradually in accordance with the increased of divergence rate. The differences among isotropic RIE etching method, directional RIE etching method and chemical RIE etching method was shown clearly in the fig.19.

Table 4: Effect of divergence rate on the threshold voltage by different etching methods. (etch rate = 33Å/Sec)

Divergence (Å/Sec)		Threshold voltage (V)		
		5	10	15
Etching Method	RIE Isotropic	0.139830	0.13983	0.13983
	RIE Directional	0.197792	0.197792	0.197792
	RIE Chemical	0.198129	0.203137	0.210151

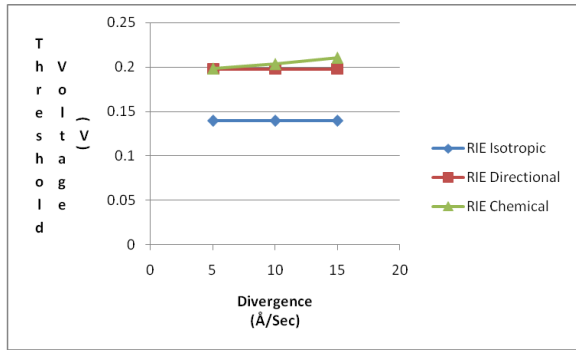


Fig.19: Effect of divergence rate on the threshold voltage by different etching methods. (etch rate = 33Å/Sec)

The comparison for all etching methods to the I_D - V_{GS} threshold voltage characteristic was shown in fig.20 and fig.21. The graph shows that the I_D - V_{GS} for directional RIE etching method and chemical RIE etching method was almost similar to the geometrical etching method. It means that the characteristic of the device was almost equivalent by using this method. On the other hand, the wet etching method and isotropic RIE etching method was absolutely different compared to the geometrical etching method. It shows that the threshold voltage for both etching methods were smaller than geometrical etching method.

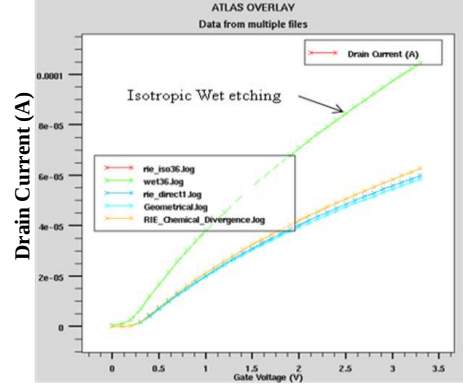


Fig.20: The comparison of different etching methods due to etch rate varying based on the threshold voltage properties.

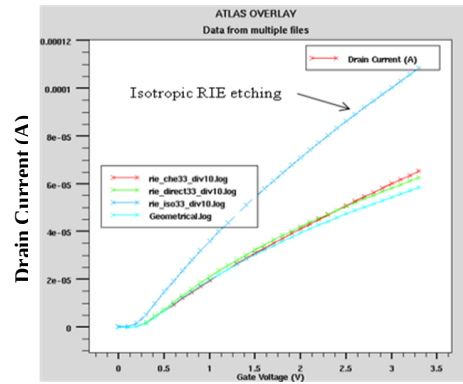


Fig.21: The comparison of different etching methods due to divergence varying based on the threshold voltage properties.

4.0 CONCLUSION

By using isotropic wet etching method and isotropic RIE etching method, the length of polysilicon was decreased by the increasing of the etch rate. The uniformity and similarity to the desired pattern of polysilicon were achieved by using the directional RIE etching method and chemical RIE etching method. The directional RIE etching method and chemical RIE etching method have usually given an anisotropic etch profile by increasing the etch rate. The chemical RIE etching method provided highly selectivity and directionality give various divergence rates. The varying of divergence rate does not affected the etch profile by using isotropic RIE etching method and directional RIE etching method. By using chemical RIE etching method, the decrement of divergence rate have changed the isotropic etch profile to anisotropic etch profile. The effect of junction depth by using all different methods was similar. The threshold voltage was rapidly increased from etch rate was 33 Å/Sec until 36 Å/Sec. The junction depth increased gradually along with the increase of etch rate. The value of

junction depth unchanged for any divergence rate by using isotropic RIE etching method and directional RIE etching method. In contrast, the chemical RIE etching methods have affected to the junction depth due to the change of divergence rate. The threshold voltage by using isotropic wet etching and isotropic RIE etching was decreased by increment of etch rate. By using directional RIE etching method and chemical RIE etching method, it was found that the threshold voltage has increased gradually by increasing the etch rate. For the isotropic RIE etching method and directional RIE etching method, the threshold voltage is not affected despite the changes of divergence. By using chemical RIE etching method, the threshold voltage was increased gradually along with the increment of divergence rate. The directional RIE etching method gives similarities with the geometrical etching method in terms of etch profile, junction depth and threshold voltage characteristic for any etch rate and divergence rate.

5.0 RECOMMENDATION

There is an alternative way to study the effect of etching process to the NMOS structure using TCAD tools. It is by using Maskview Interface of Athena Silvaco. The Maskview is a Virtual Wafer Fab (VWF) Interactive Tools of Silvaco's software. This software is designed specifically for interfacing IC layout information with process and device simulators. The Maskviews have facilitates to create a complicated masks layout.

ACKNOWLEDGEMENTS

With the highest praise to Allah which gives the author the energy and spirit to complete this project successfully. The author would like to express sincere appreciation and gratitude to En Uzer Md Noor as the respective supervisor and Assoc. Prof. Dr. M. Rusop as a co-supervisor for this research. Special thanks to the lecturers and management of Faculty of Electrical Engineering, UiTM. Not to forget, to all research members at Solar Cell Lab for giving their hand and ideas in making this project a success. Without their generosity, this research would not be possible to complete. Last but not least, deepest appreciation to the author's family for the faith instilled as a step in manoeuvrings this life.

REFERENCES

- [1] Silvaco International, "ATHENA User's Manual 2D Process Simulation Simulation Software", February 2000.
- [2] Syafeeza binti Ahmad Radzi, "Simulation of 0.18 Micron MOSFET and its Characterization", Faculty of Electrical Engineering, Universiti Teknologi Malaysia, Thesis of Degree, Master of Engineering, October 2005.
- [3] D. Andriukaitis, R. Anilionis, "Investigation of Etching Process in Nano Structures", Department of Electronics Engineering, Kaunas University of Technology, ISSN 1392 – 12152008, Nr. 6 (86).
- [4] Scott Thompson, Paul Packan, Mark Bohr, "MOS Scaling: Transistor Challenges for the 21st Century", Intel Technology, Journal Q3, 1998.
- [5] Betty Lise Anderson, Richard L. Anderson, "Fundamentals of Semiconductor Devices", McGRAW HILL, International Edition, 2005, p385-p434.
- [6] Richard C. Jaeger, Volume V: Introduction to Microelectronic Fabrication, Prentice Hall, Second Edition, 2002, p25-p30.