UNIVERSITI TEKNOLOGI MARA

DESIGN OF ULTRA LOW-POWER, WIDE-BAND OPERATIONAL AMPLIFIER USING THE PROGRAMMABLE MOS DEVICES

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ABSTRACT

The direction towards lowering supply voltages and power consumption presents new challenges in the design of electronic circuits of high performance. Each new generation of electronic equipment integrates more functions into a single integrated circuit to meet the growing demands of electronic applications. Therefore, there is a need to present new techniques for reducing power consumption in the design of such circuits. In the design of integrated circuits such as the two-stage CMOS operational amplifier, the power consumed should be reduced as low as possible, considering the optimization of other parameters such as stability, bandwidth, slew rate, and output swing to achieve a near-ideal performance. Although the two-stage CMOS operational amplifier has a higher voltage gain and relatively wider bandwidth, it suffers instability unless it is processed by external frequency compensation techniques such as Miller compensation or through adding a voltage buffer or current buffer in series with a compensation capacitor. In addition, it exhibits a non-constant transconductance over the common-mode input range and then an imperfect output swing, even if its input stage is a rail-to-rail. External frequency compensation techniques create a trade-off between stability and bandwidth. Additionally, the non-constant transconductance leads to voltage gain instability across the common-mode input range, reducing the output swing. Therefore, a new approach is presented in this thesis to design a CMOS two-stage operational amplifier that operates within an ultra-low power supply and features a near-ideal performance of other parameters. The new approach adopts two types of technologies: self-compensation instead of external compensation techniques and stable bias currents along the common mode input range. The self-compensation technique is attained by using the electrical programming technology for the MOS devices to obtain high transconductance, wide bandwidth, and high slew rate while operating at ultra-low power range. The use of stable bias currents is to stabilize the overall transconductance to guarantee the typical rail-to-rail operating along the common-mode input range. In addition, using electrical-programmed MOS devices that featured near-ideal structural matches revealed that the operational amplifier behaves ideally in rejection of the common-mode input and power supply variations. Simulation results show that the new design achieves 35.5% lower power consumption, and 65.5% upper bandwidth.

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CHAPTER 1
INTRODUCTION

1.1 Research Background

Operational amplifiers (op-amps) usually have three terminals: two inputs, which are the inverting and non-inverting terminals, and output terminal. Op-amps are considered the backbone of a variety of analog applications, such as signal processing, electronic control, mathematical operations, and so on. Typical applications of op-amps include non-inverting amplifiers, inverting amplifiers, and voltage followers. There are several ways to categorize the op-amps: for example, they are classified based on the power supply as single supply and dual supply, based on the input circuit as P-type differential amplifier or N-type differential amplifier or rail-to-rail stage, and based on electrical characteristics; as a low input offset, low power consumption, and low noise.

Since the op-amps are analog circuits, the design of these devices requires an understanding of the analog fundamentals, such as loading, frequency response, stability, and power consumption. The low-power applications in analog circuits heavily depend on the power consumption in the op-amps. Therefore, in the design of the op-amps, low voltage, low power consumption, and high gain should be taken into account with considering the improvement of other parameters such as stability, bandwidth, slew rate, and output swing.

1.2 Low-Voltage and Low-Power Limitations

When designing a low-power op-amp, some essential limitations should be considered without compromising the speed. These limitations such as, reducing the power supply voltage, reducing the threshold voltage and increasing the transconductance, affect the output swing, stability of the op-amp, and the bandwidth.

1.2.1 Power Supply Voltage

One of the methods used to reduce the power consumption when designing a low-power op-amp is reducing the power supply voltage. Reduction of the supply