A RF-Low Power 0.18-μm CMOS Based Differential Ring Oscillator

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*Abstract~***The paper present the design of oscillator in general using ring oscillator for analysis of a low power voltage controlled ring oscillator, wide range of frequency and low phase noise analysis, as a main 3 objective of this paper. This work has been implemented using gateway simucad empowering using silvaco eda tool software ,this circuit also implements in 0.18µm technology. The design is based on 3 stages of the ring oscillator due to modification of improvement control voltage source(V_{ctrl}) and tail current (V_{tail}).A tail current improvement is responsible to control the charging and discharging time of oscillator. Diffrential delay cell stages improvement are functionally as a noise reduction.The output of frequency is in between 0.73GHz and 3.52GHz with control voltage of 1V to 1.8V.The phase noise simulation result is-90.15dBc/Hz and the circuit drawn 6.59mW of power at Vtail=Vctrl=1V and the circuit drawn7.61mW of power at Vtail=Vctrl=1.8.**

Keywords-low power ,phase noise, tail current ,differential delay cell ,tail current

I. INTRODUCTION

The Oscillator is an electronic circuit that produces repetitive,oscillating electronic signal,often a sine wave or square wave.In radio frequency, lightwave communication systems and wireless communication system,oscillators are used for frequency translation of signals and channel selection.Oscillator also presents in all digital electronic systems,which require a time reference,i.e. a clock signal,in in order to synchronize operation.

In a modern wireless communication nowadays, VCO is a main role and essential components to this operating system.The good VCO is depends on the low phase noise,low power consumes and high frequency swing[1].They are mainly have two type of VCOs , ring oscillator and LC tank.For the ring oscillator it have wide tuning range with low power and small layout design areas,but with relatively poor phase noise[2].But the phase noise requirements are decreased in some applications of short-range communications,data rates are low,and the channel spacing wide[3].For this proven in the ring oscillator it can see that to make the voltage controlled ring oscillator is widely applied which needs smaller chip area and has a large tuning range compare than LC oscillator.For LC oscillator it has low phase noise but low tuning range frequency.

In the last paper that is a LC oscillator has a weakness that need to upgrade and improvement that is proposed in this paper, the information about the LC oscillator can be explained in figure 1 below.

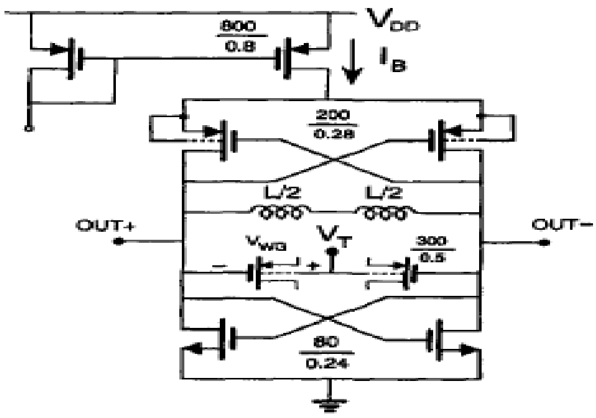

Figure1:LC oscillator schematics[4]

Fig. 1[4] shows the oscillator schematic. The appropriate tuning range and phase noise are the *two* primary design specifications. A 2.5 V maximum voltage on chip limited by breakdown conditions is assumed. The output frequency must cover 4.8-4.96 GHz over all process variations. Assuming a + 10% tank component variation, the tuning range with respect to the 4.9 GHz central frequency, is 14%. When the VCO is embedded in a PLL and the tuning node is driven by a charge pump, the theoretical limits of the *VT* swing are 2.5 V maximum and 0 V minimum. However, the open-loop high gain conditions restrict this range to about 2.2-0.3 V[4]. The maximum noise-to-signal ratio (SSCR) at 1 MH offset from the carrier is desired to be -108dBc/Hz over the whole tuning range.

This paper presents a three stage of ring oscillator is design using 0.18µm CMOS technology using silvaco gateway and the result is using simucad analysis software. The circuit is improvement with tail current to achieve an RF frequency range as a for compared with control voltage to get the high frequency tuning range ,low power analysis and low phase noise. The circuit is build in three stage ,for the first stage it consists differential CMOS NAND gate and the other two delay cell is using differential CMOS inverters.The NMOS for the tail current is added at the differential CMOS NAND gate. The input for the first delay act as a control voltage for implement the tuning range of the frequency.

II. DESIGN OF RING OSCILLATOR

A. *Flow Chart of the Project*

The design step of the Proposed Ring Oscillator is shown in Figure 2.

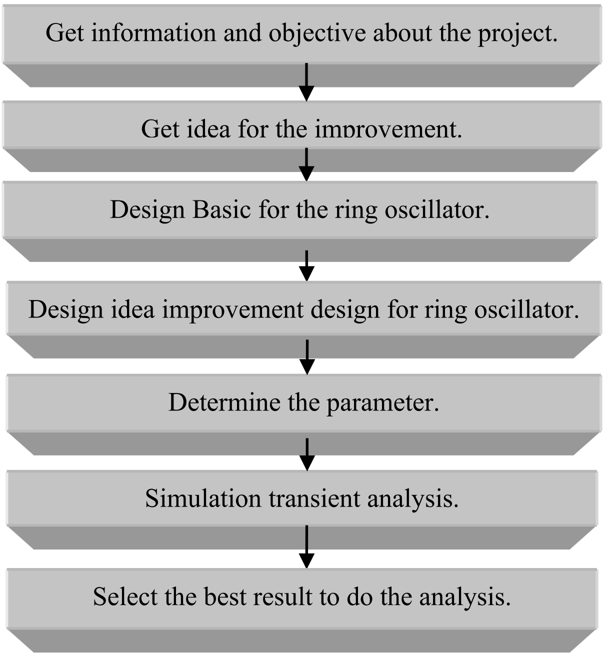

Figure 2:The design step of the Proposed Ring Oscillator

In the figure 2 show the flow chart of the step in doing this ring oscillator until get the result that has just been explained in the abstract. For the first of the step,the information about the circuit, theoritical about the circuit must take as a import role in doing this design and then read the literature review about the past project. For the next step get idea for the improvement of the circuit and the improvement for this design is with the additon tail current and use differential CMOS gate as to get the best result comparing with other paper has just been doing for example in LC circuit ,VCO amberker and others circuit that can be explained in the result part. Design basic ring oscillator for the next step is to know about basic operation of ring oscillator.

After that, design the actual ring oscillator with the improvement of the design ,the design for this circuit is using gateway silvaco eda tool software, with the new design the next step is to determine the parameter in the circuit for example W and L for the PMOS and NMOS. After the design and with no error in the circuit, next is simulate the design to get the result.The simulation of this result is using simucad analysis in silvaco software. For the last step of this project, do the analysis with the creteria that needed for this design.

B. *Proposed of Ring Oscillator*

1) *Tail Current Improvement*

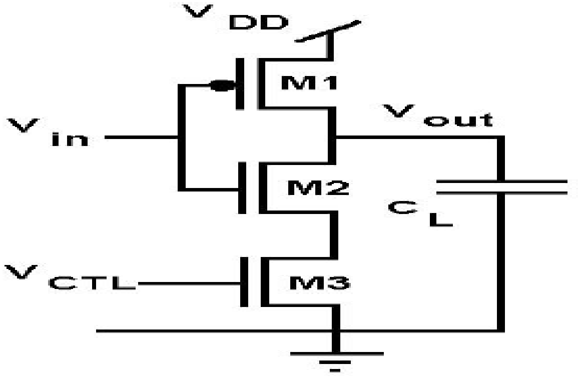

Figure3:Tail current improvement

The tail current improvement is shown in the figure 3[5].The basic concept for this tail current is to reduce charging and discharging time for this design. The new transistor M3 is added as a current source to transistor M1 and M2.This concept of tail current is when Vin<VtM1,M2 is turn off and M1 is turned on.The VDD charge output node capacitance through M1 and M3.For this case it can reduce the charging time for the inverter compare from the normal inverter case,Vt is represents the threshold voltage for particular transistor.

For the discharging case, when Vin>Vt,M2 is turned on and M1 is turned off,output node capacitance is discharging through the M2 and M3where M3 provide discgarging current as soon compare to M2 ann M1 in situation turn off. The initial discharging current reduce the discharging time for the output node capacitance CL.

2) *Differential Delay Cell Improvemrnt*

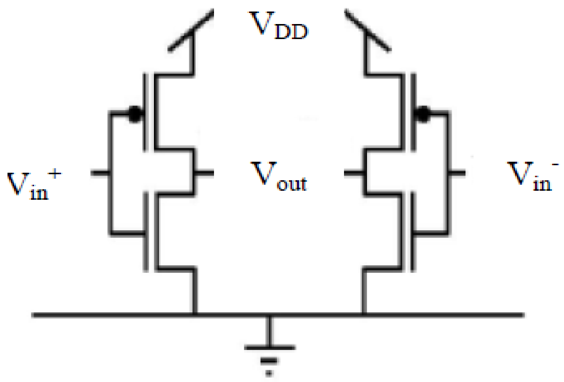

Figure 4:Basic differential delay cell improvement

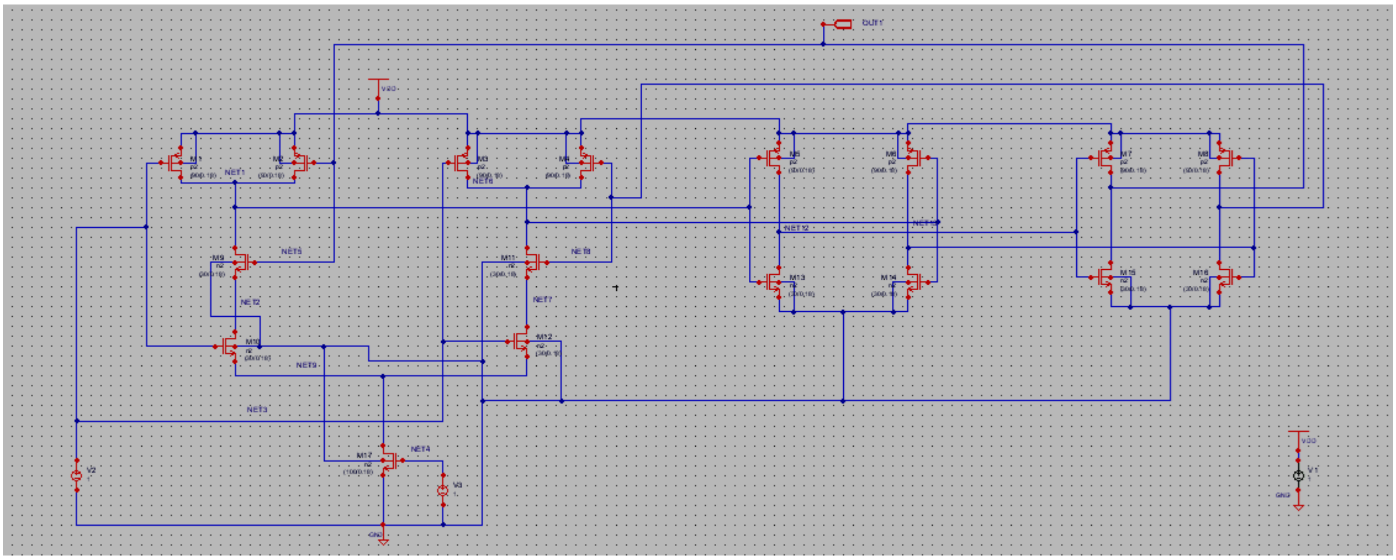

Figure 5: Proposed 3 stage differential cell

A basic differential delay cell is shown in figure4[5].Differential delay cell.The differential delay cell rejects the commom mode and power supply noise and improves the noise performance[6].The major differentially between single ended and double ended is it has two differential input as compared to single. In the differential configuration a last differential buffer stage can be added to odd number of delay stages,if the output is not stable,this will create an even stages[6].

In this paper,a three stage differential voltage control is used as a voltage controlled.No last differential buffer is used.Power consumption will increase with number of componenets transistor,thus least three stages are used.

C. Ring Oscillator Circuit and Design

The schemetics shown in figure 5 is a actual design ring oscillator after improvement from the figure 3 and figure 4.The first delay cell is CMOS differential NAND gate and the other delay cell is CMOS inver differential.The first delay cell will act as a inverter if the input are same.Each inverter has a certain delay between stages.This delay is termed as ‘inverter pair delay’.

1) Frequency Related Issues Analysis

As shown in figure 5,each delay cell has an ‘inverter pair delay’.This is defined as the sum of the total of rise time and fall time of the individual inverter stages[5],for example N-stage ring oscillator the oscillation frequency is defined as[5].

$$Fosc = \frac{1}{N(trise + tfall)} \qquad (1)$$

Where, Fosc is the frequency of oscillation,N is number of stages and $t\,rise, t\,fall$ are the rise time and falling time of each delay cell respectively.For good VCO and ideal for ring oscillator $t\,rise = t\,fall = t$,the frequency oscillation is defined as[6]:

$$Fosc = \frac{1}{2Nt}$$

As 3 stage ring oscillator oscillators are presented in this paper so,N=3,the new formula for frequency oscillation is convert to:

$$Fosc = \frac{1}{6t} \qquad (2)$$

The equation (2) is the time domain analysis for ring oscillator.That is comfirmed ,the equation for ring oscillator depends on number of stages(N).If the number of stages are more the overall delay increases,which results in diminishing of the frequency of overall system.Actually,there is a trade-off between number of stages and frequency of the oscillator.So, for high frequency applications it is necessary to design such type of oscillator which has minimum number of stages[7].

2) W/L Related Issues Analysis

For the inverter shown in fig 6,the (W/L) ratios of the transistors (nMOS and pMOS) are given as[8].

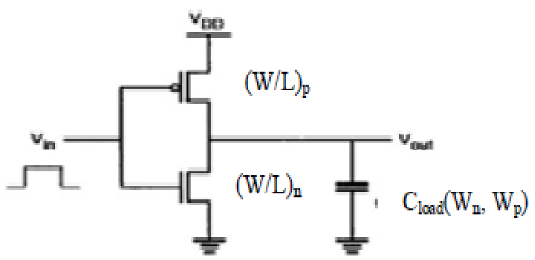

Figure 6:CMOS Inverters

Now consider the W/L aspects for the proposed design. For the simple CMOS inverter,The ratio of transistor (nMOS and pMOS) defined as $(W/L)_n$ and $(W/L)_p$ respectively and the total load capacitance is defined as C_{load}[8].

$$\left(\frac{W}{L}\right)n = \left[\frac{\text{Cload}}{t\,fall\ \mu n\ Cox\ (Vdd - Vtn)}\right] \left[\frac{2Vtn}{Vdd - Vtn} + ln\left(\frac{4(Vdd - Vtn)}{Vdd} - 1\right)\right] \quad (3)$$

$$\left(\frac{W}{L}\right)p = \left[\frac{\text{Cload}}{t\,fall\ \mu p\ Cox\ (Vdd - Vtp)}\right] \left[\frac{2Vtp}{Vdd - Vtp} + ln\left(\frac{4(Vdd - Vtp)}{Vdd} - 1\right)\right] \quad (4)$$

Where C_{load} is the output load capacitance and C_{ox} is the gate oxide capacitance per unit area.Again taking $t\,rise= t\,fall= t$, equation (3) and (4) will be as:

$$\left(\frac{W}{L}\right)n = \left[\frac{\text{Cload}}{t\ \mu n\ Cox\ (Vdd - Vtn)}\right] \left[\frac{2Vtn}{Vdd - Vtn} + ln\left(\frac{4(Vdd - Vtn)}{Vdd} - 1\right)\right] \quad (5)$$

$$\left(\frac{W}{L}\right)p = \left[\frac{\text{Cload}}{t\ \mu p\ Cox\ (Vdd - Vtp)}\right] \left[\frac{2Vtp}{Vdd - Vtp} + ln\left(\frac{4(Vdd - Vtp)}{Vdd} - 1\right)\right] \quad (6)$$

Clearly as $\mu_p<\mu_n$,the $(W/L)_p$ will be greater than $(W/L)_n$.

3) Power Related Issues

As the low power consumption based devices are more reliable[9],power consumption plays a significant role in CMOS design. Power consumption is reduced by proper selection of logic and architecture.Power consumption of CMOS device depends on several factors such as input voltage, density of circuit, operating frequencies ,output loadings and capacitances of device. Power consumption is measured using supply voltages,current in devices,selection of device and operating frequency[1].

The static power consumption of the CMOS inverter is quite negligible.During switching events where the output load capacitance alternatively charged and discharged,the CMOS inverter concumes power[8].

Considering figure 7 and assuming that the input is an ideal voltage waveform with negligible rise and fall time.

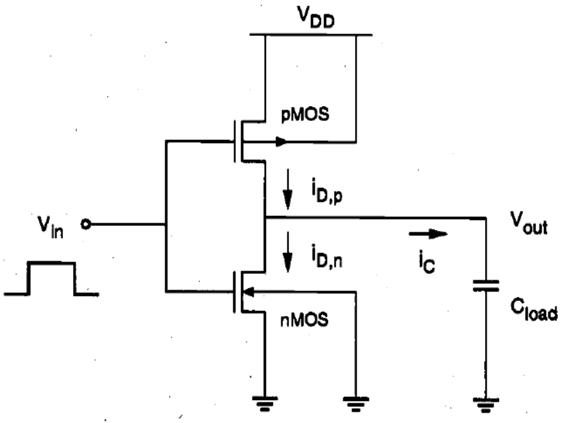

Fig 7.CMOS inverter for power analysis[15]

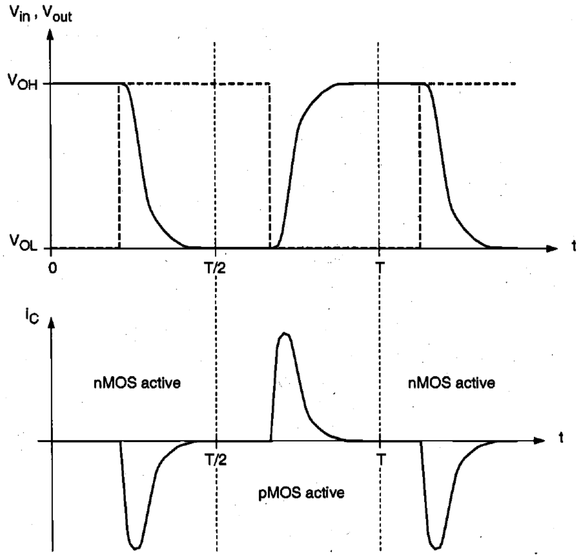

Fig 8:Input and Output voltage and capacitor current waveform[15]

From figure 7,8 and assuming periodic input and output the average power consumed over one period is given as:

$$Pavg = \frac{1}{T}\int_0^T v(t).i(t)dt \quad (7)$$

The pMOS and nMOS conduct current for half period each thus:

$$P_{avg} = \frac{1}{T}\left[\int_0^{T/2} Vout\left(-Cload\ \frac{dVout}{dt}\right)dt + \int_{T/2}^{T}(Vdd - Vout)\left(Cload\frac{dVout}{dt}\right)dt\right]$$

Evaluating the integrals we get:

$$P_{avg} = \frac{1}{T}Cload\ Vdd^2 \quad (8)$$

As $F_{osc} = \frac{1}{T}$

$$P_{avg} = C_{load} . Vdd^2 . F_{osc} \tag{9}$$

4) *Phase Noise Related Issues Analysis*

As we know, phase noise performance of ring oscillator is poored than LC resonator based oscillator[10].Phase error introduced by noise impulses is highest at the waveform rising and falling edges where energy is being pushed into or pulled from the load capacitors. The comparison that make ring oscillator is poored than LC oscillator is in LC oscillator the capacitor charged is not completely removed per cycle but in case for ring oscillator complete charging and discharging is occured in the node of capacitance.Figure 9[10] shows the amplitude and phase noise on oscillator signal.

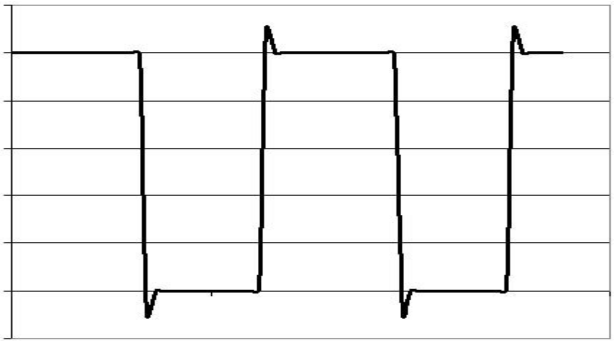

Figure 9 Amplitude and Phase noise on oscillator signal[17].

Analysis has shown,that single ended ring oscillators exhibit a relatively constant amount of phase noise independent for the number of stage N for a given frequency and power consumption[10]:

$$PN = \frac{16kt}{3Pdc}\left(\frac{Fosc^2}{\Delta F}\right) \tag{10}$$

Where Pdc is power consumption ΔF is an offset frequency close to oscillation frequency.

III. Simulation Results and Discussions

1) *Similation Results.*

The schematic shown in figure 5 is designed and simulate using gateway silvaco edatool using 0.18µm CMOS technology and the output response are plotted using simucad transient analysis.

Figure 10 shows the transient response at V_{ctrl}=1v and V_{tail}=1v with oscillation frequency F_{osc}=0.73GHz.Similarly for figure 11,the transient response at V_{ctrl}=1.8v and V_{tail}=1v and the raeding of F_{osc} is given 3.326GHz.In the figure 12,the result shown F_{osc}=1.76GHz from the value V_{ctrl}=1v and V_{tail}=1.8v and the figure 13 shows V_{ctrl}=1.8v and V_{tail}=1.8v with oscillation frequency,F_{osc}=3.52GHz.

From the explaination detailed in the frequency oscillation shows,the minimum oscillation frequency is 0.73 GHz at V_{ctrl}=1v and V_{tail}=1v,and the maximum oscillation frequency is 3.52GHz at V_{ctrl}=1.8v and V_{tail}=1.8v.So,as a result this oscillator work in between 0.73GHz and 3.52GHz in a range2.73GHz.

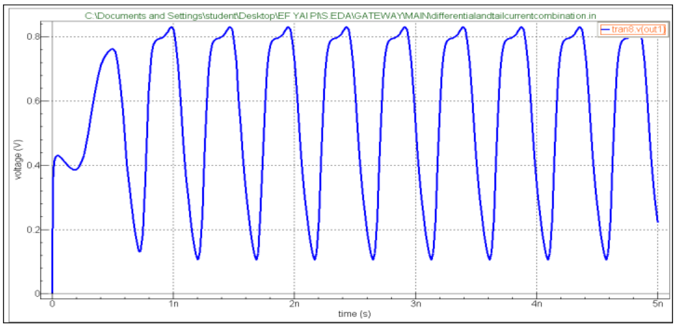

Figure 10 Transient response V_{ctrl}=1v,V_{tail}=1v,F_{osc}=0.73 GHz

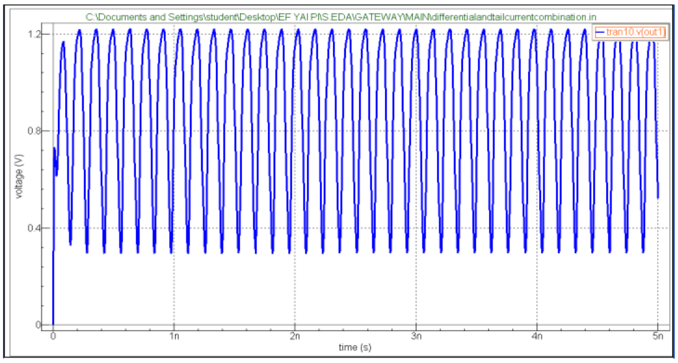

Figure 11 Transient response V_{ctrl}=1.8v,V_{tail}=1v,F_{osc}=3.326 GHz

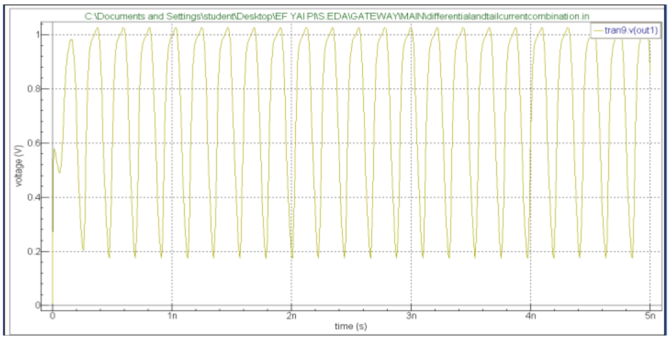

Figure 12 Transient response V_{ctrl}=1v,V_{tail}=1.8v,F_{osc}=1.76 GHz

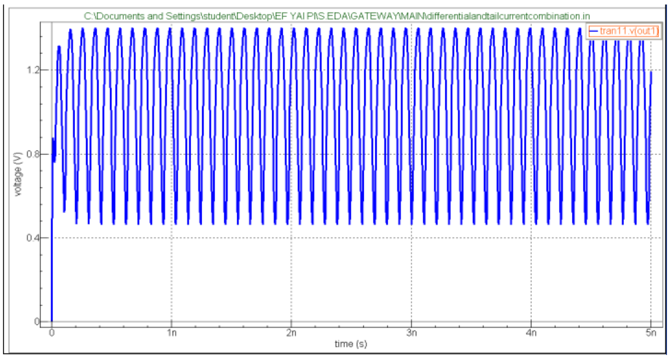

Figure 13 Transient response V_{ctrl}=1.8v,V_{tail}=1.8v,F_{osc}=3.52GHz

Figure 14 and 16 shows a transient power for the minimum and maximum oscillation frequency respectively and figure 14 and 16 shows the result of average power read from the transient power.In figure 14 the minimum oscillation frequency for 0.73GHz show the average power is 6.59mW and for the result of average power in maximum as oscillation frequency 3.52GHz,the result of average power is 7.61mW.

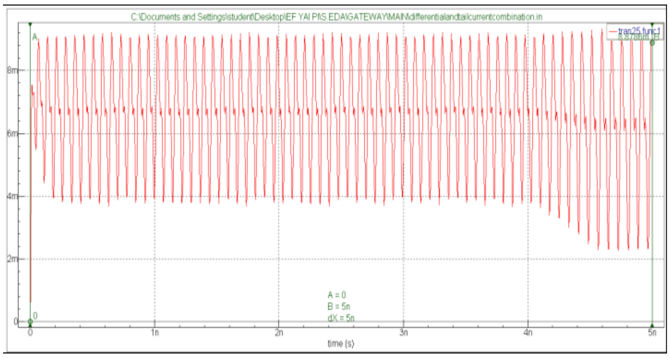

Figure14 Transient power at V_{ctrl}=1v,V_{tail}=1v

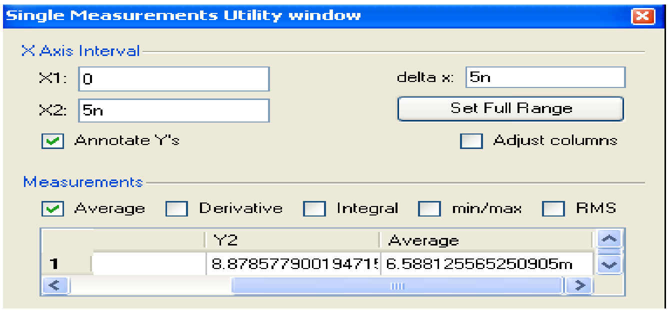

Figure 15 Transient power at V_{ctrl}=1v,V_{tail}=1v =6.59mW

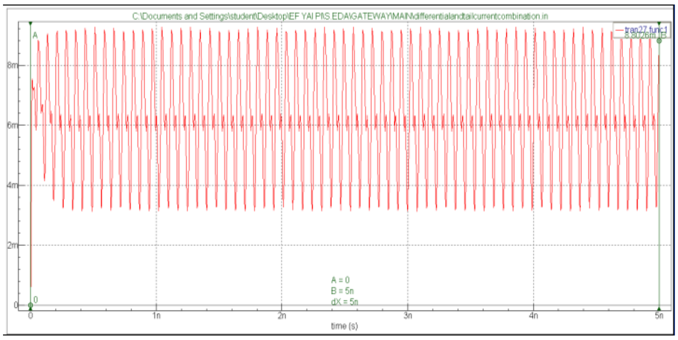

Figure16 Transient power at V_{ctrl}=1.8v,V_{tail}=1.8v

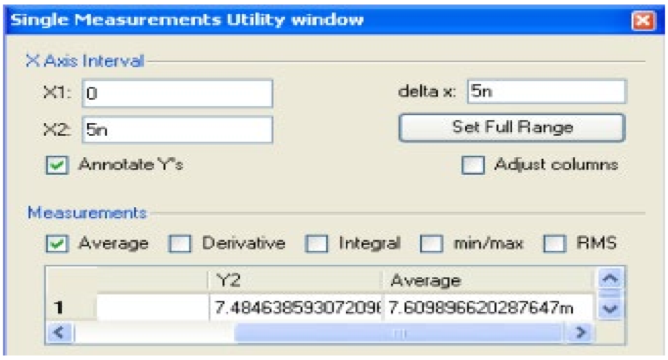

Figure 17 Transient power at V_{ctrl}=1.8v,V_{tail}=1.8v=7.61mW

Figure 18 shows the noise response at V_{ctrl}=V_{tail}=1v with phase noise -80.98dBc/Hz@1MHz.Similarly figure 19 shows noise response at V_{ctrl}=V_{tail}=1.8v with phase noise -90.17dBc@1MHz.

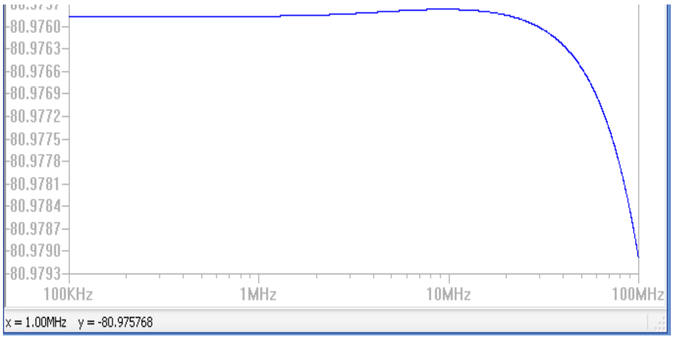

Figure 18: Transient response V_{ctrl}=V_{tail}=1V,PN=-80.98dBc/Hz@1MHz

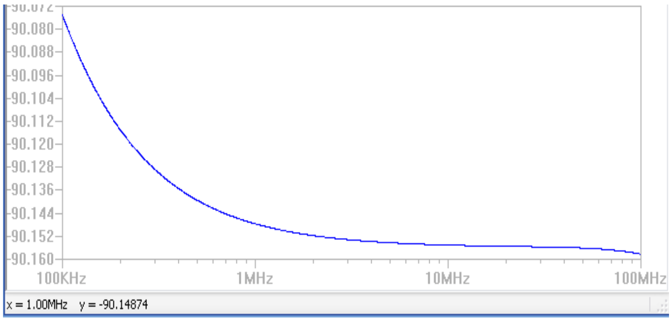

Figure 19: Transient response V_{ctrl}=V_{tail}=1.8V, PN=-90.15dBc/Hz@1MHz

2) Analysis Data

Case 1:Power vs Frequency Relation: Here it clearly seen that in the propose design of this oscillator,since the frequency is increase the power dissipation is also increase.The result is also can be conclude that oscillator power is directly proportional to the frequency.

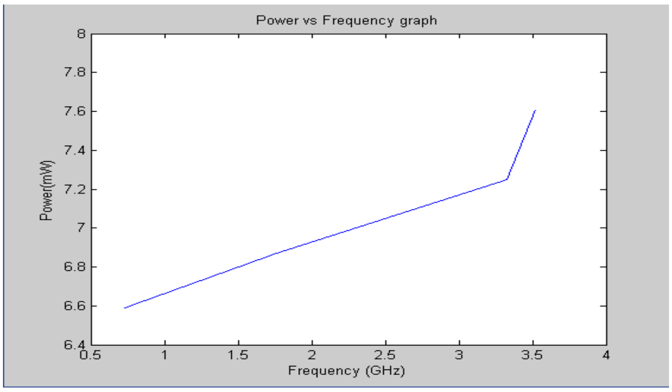

Figure20:Frequency vs Power Graph

Case 2:Voltage vs Frequency at fixed variable voltage: Figure 21 shows the experimental of this proposed ring oscillator relationship between frequency and control voltage at fixed tail voltage.It is assumed that tail current transistor is always in the saturation region.It is clearly seen that in figure 21,control voltage increase,the frequency is also increases linearly up to its maximum 3.52GHz.In the other hand, figure 22 shows the relationship between frequency and tail voltage.The relationship also seen the frequency is also directly proportional to the increase of tail voltage. From the two graph, it can be conclude that the minimum and maximum of oscillation frequency can be 0.73GHz and 3.52GHz respectively. So as a conclusion,tuning range is in between 0.73GHz and 3.52GHz.

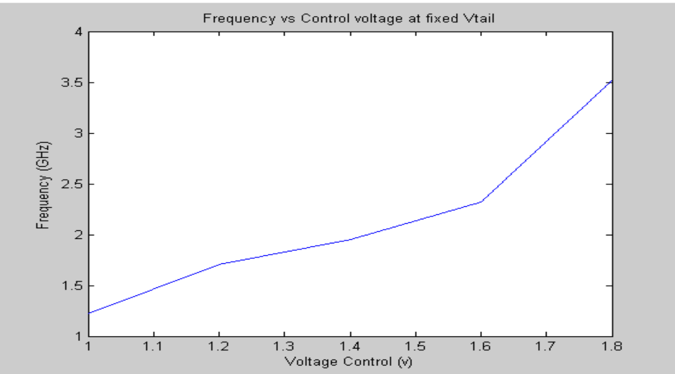

Figure 21:Frequency vs V_{ctrl} at fixed V_{tail}

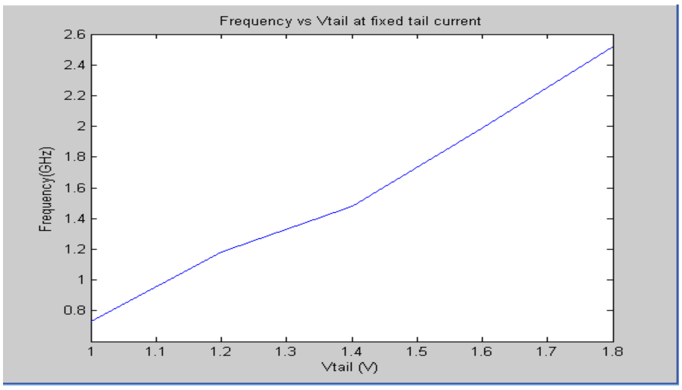

Figure22:Frequency vs V_{tail} at fixed V_{ctrl}

Case 3: Relationship of two Case 2 analysis to the tuning range: From the combination of figure 21 and figure 22,it can produce one graph that tell relationship between frequency and voltage in this proposed ring oscillator.Figure 23 shows the tuning voltage relationship with the frequency oscillation.

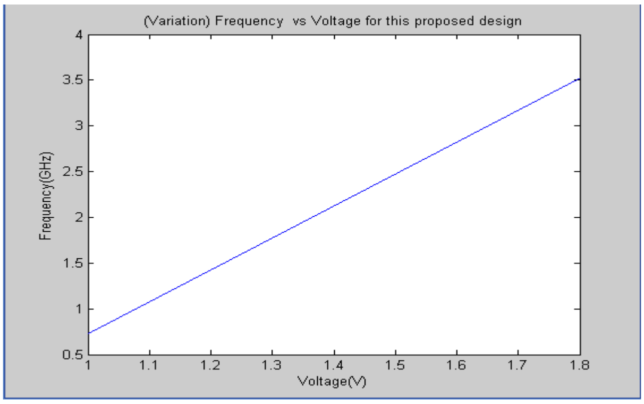

Figure 23:Frequency oscillation vs voltage

3) Performance Comparison

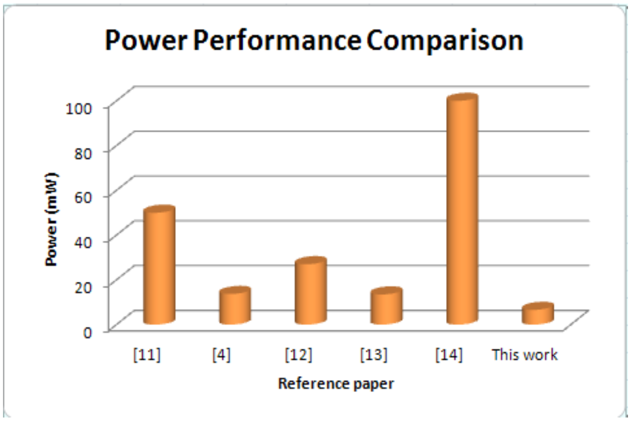

Figure 24 Power Performance Comparison

From the analysis in figure 24 above, have seen that that power performance comparison between this proposed paper with the other paper that have been refer as a literature review from the past paper.As a reference,the other paper comparison can be seen in table 1 below .As a conclude in this figure 24,seen that this proposed paper produce low power consumption than other paper with 6.59 mW and the highest power that be seen is in reference[11] with 100mw.So, the main objective for this project is achieved.

TABLE 1 :PERFORMANCE COMPARISON

Reference	Process Technology(µm)	Type	Tuning Range (GHz)	Power (mW)	Phase Noise dBc/Hz@1MHz	Supply Voltage (volts)
[10]	0.18µm	Ring	8.4-10.1 (1.7 B.W)	50	-99.9	1.8
[11]	0.25µm	LC	4.55-5.45 (0.9 B.W)	13.7	-114	1.8
[12]	0.18µm	Ring	5.16-5.93 (0.77 B.W)	27	-99.5	1.8
[13]	0.18µm	Vacker VCO	4.85-4.93 (0.08 B.W)	13.5	-	1.8
[14]	0.18µm	Ring	3.03-5.36 (2.33 B.W)	100	-	1.8
This work	0.18µm	Ring	0.73-3.52 (2.79 B.W)	6.59	-90.15	1.8

IV. CONCLUSION

In this paper 3 stage of ring oscillator design is demonstrated and implemented using 0.18µm CMOS technology using gateway silvaco edatool.By using two tuning voltage source (i.e V_{ctrl} and V_{tail}) and with the minimum numbers of delay cell in the result of wide range of frequency is achieved between 0.73GHz-3.52GHz.In other ways, the low power consumption 6.59 mW is achieved by minimized the number of transistor in the proposed design.The phase noise of this design can be -90.15 dBc/Hz@1MHz.The attractive feature of this paper is to minimize the the trade-off between frequency and power consumption is established.The comparison between this proposed design and the other paper that can be seen in table1.So,this proposed ring oscillator can be used for wide range of RF low power applications such as wireless communications,clock recovery system and low power high frequency applications.

ACKNOWLEDGMENT

The authors would like to express his gratitude to Madam Wan Rosmaria Bt Wan Ahmad for her thoroughly supervision and support in completing this work. Not to forget,the faculty of Electrical Engineering Universiti Teknologi Mara(UiTM) for providing the good environment and facilities for research and study.

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