Implementation of Sinusoidal Pulse Width Modulation Based on CORDIC Algorithm using Silterra 0.18 µm CMOS Technology

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Abstract–**This paper presents the implementation of back-end design for Sinusoidal Pulse Width Modulation (SPWM) using Silterra 0.18µm technology and it is based on CORDIC algorithm. The SPWM technique is used to control switches such as Insulated Gate Bipolar Transistor (IGBT) in major AC appliances. Synopsys tool is used to synthesize the Verilog Hardware Description language (HDL) model of the SPWM to its ASIC form. The use of Coordinate Rotation Digital Computer (CORDIC) in the source code make it provides an area-efficient architecture for effective design at Silterra 0.18µm CMOS technology.**

Index Tern **– Sinusoidal Pulse Width Modulation (SPWM), Coordinate Rotation Digital Computer (CORDIC), Insulated Gate Bipolar Transistor (IGBT), Synopsys.**

I. INTRODUCTION

Pulse Width Modulation (PWM) is normally used as a controller in power conversion and motion control. There are various kinds of modulating modes available such as sinusoidal PWM, space vector PWM, current tracking PWM, harmony elimination PWM and others [1]. The most widely used in industrial applications are the sinusoidal PWM and space vector PWM [2]. The SPWM is used to control the insulated gate bipolar transistor (IGBT) which is a three-terminal power semiconductor device with high efficiency and fast switching. They are normally used in applications such as electric cars, air-conditioners and stereo systems that switch rapidly [5]. SPWM produces several pulses per half cycle. The pulses near the edge of the cycle are always narrower than the pulses near the center of the half cycle such that the pulse widths are proportional to the corresponding amplitude of a sine wave at the portion of the cycle [3]. The conventional SPWM uses lookup table method in generating sine wave signal but it is not effective in area-architecture hardware implementation due to excessive memories needed if better resolution is used.

CORDIC is another method in generating trigonometric functions such as sine, cosine, sinh and cosh. It is an acronym for Coordinate Rotation Digital Computer. Since the objective of this project is to generate SPWM signal and the reference signal to be compared with the triangular wave in SPWM is sinusoidal signal, hence, only sine function is considered. Thus, the architecture for CORDIC algorithm and its hardware is only based on the sine function.

This paper describes the operation and the implementation of SPWM using Silterra 0.18um CMOS technology. The design is synthesized to its IC layout by Astro. It is a Synopsys tool commonly used in ASIC industry. Capacity limits and excessively long run time are major application issues of the physical synthesis tools in multi-million gate designs. Consequently, large designs often resort to hierarchical physical implementation methods [6].

II. SINUSOIDAL PULSE WIDTH MODULATON

A. *CORDIC Architecture*

The sine function is a class of shift and additional algorithms for rotating vectors in a plane [4] as given

$$\begin{pmatrix} \cos\theta & -\sin\theta \\ \sin\theta & \cos\theta \end{pmatrix} \begin{pmatrix} x \\ y \end{pmatrix} = \begin{pmatrix} x' \\ y' \end{pmatrix} \quad (1)$$

(where (x' ,y') are the coordinates of (x, y) rotated by the angle of ϑ).

The sine and cosine function using rotation mode has a rotation of è, has coordinates of (cos θ, sine θ). This implies that if a point on the x-axis is rotated by an

angle θ, then the sine and cosine of the angle of rotation may be read directly off the x and y axis. The vector rotation may be achieved by rotating the point on the unit circle in a series of steps, which are smaller than θ. The CORDIC Architecture is shown in Fig.1.

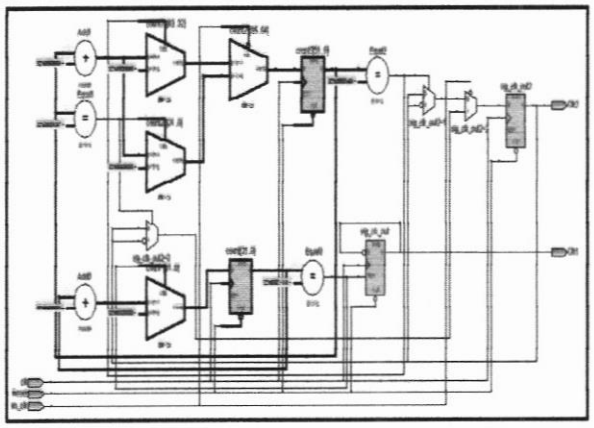

Fig.1: CORDIC Architecture

B. *Concept of SPWM output*

The sinusoidal pulse width modulation (SPWM) produced by comparing between triangular waveform, V_c, and sine waveform, V_{ref}. The Sine waveform also called as reference signal and the triangular waveform called as carrier signal. The cross over point between triangular waveform and sine waveform will generate the pulse width. The output SPWM is illustrated in Fig.2.

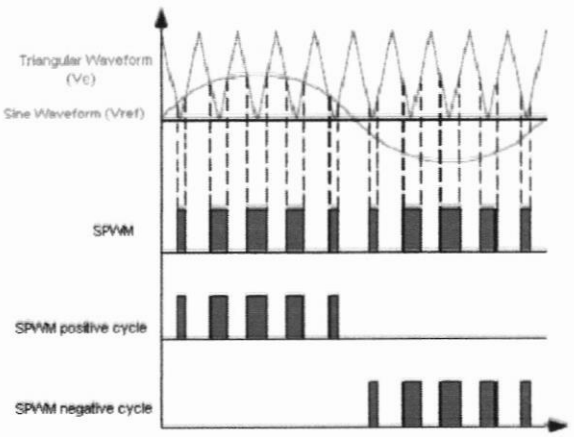

Fig.2: Formation of SPWM

When sine waveform, V_{ref}, is greater than triangular waveform, V_c, the pulse width will start high and it comes to low when the sine waveform lowers than triangular waveform.

III. METHODOLOGY

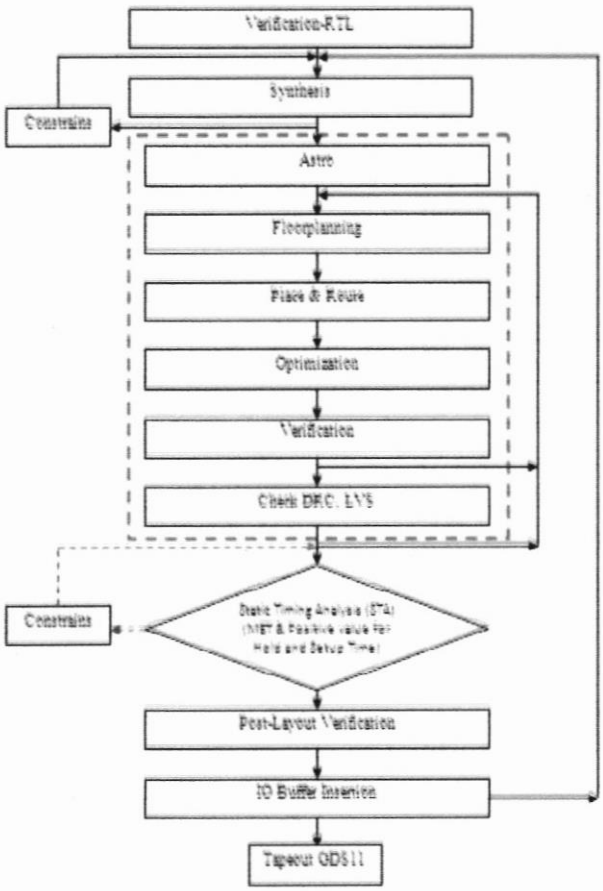

Fig.3: process in developing the IC layout.

A. *RTL Verification*

The architecture for SPWM as shown in Fig.1 has been modeled using Verilog language and it has been simulated and verified by Modelsim and VirSim. The Register Transfer Logic (RTL) verification is the starting point of back-end design. The RTL is simulated and synthesized before performing the layout (floorplanning, place and route). Static Timing Analysis (STA) has to be done before and after the layout in order not to violate any timing constraints.

Fig.4 and Fig.5 illustrated the RTL simulation and synthesizable RTL performed by VirSim.

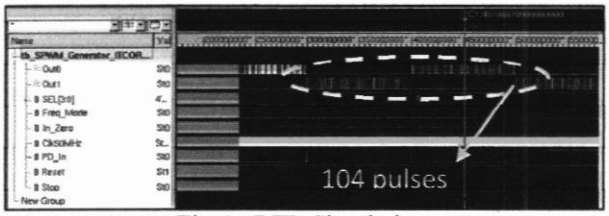

Fig.4: RTL Simulation

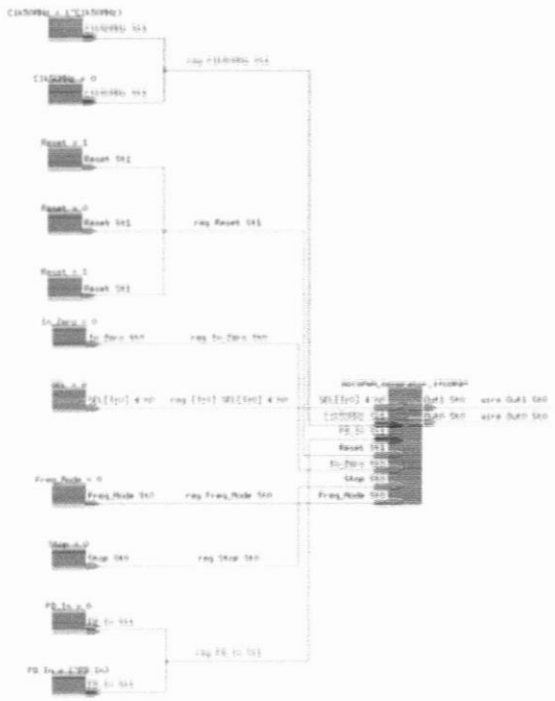

Fig.5: Register Transfer Logic (RTL)

B. *Floorplanning*

A quality synthesis result is important to a successful timing closure. Physical Compiler based synthesis flow optimized this design. The gate level is the result when performing the logic synthesize in the design compiler where the used of constrain and RTL code. The timing report for hold and setup time have to MET in positive value. Astro is a Synopsys tool that perform layout of the design. Floorplan of integrated circuit (IC) is representation of tentative placement of its major functional blocks and are created during the floorplanning design stage, an early stage in the hierarchical approach to chip design. The layout planner provides functionality to estimate area and interconnect parasitic. Fig.6 illustrated the floorplan for SPWM.

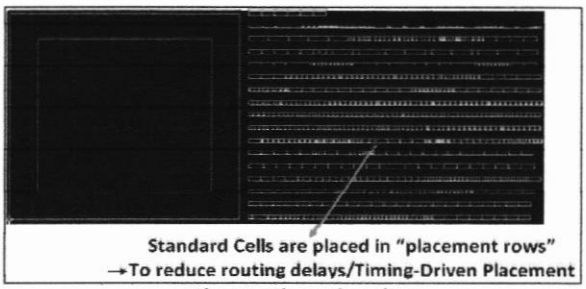

Fig.6: Floorplanning

C. *Place and Route (P&R)*

Layout is built out of three type of reference cells which is Macro cell (ROMs, RAMs), Standard Cells (nand, inv, dff) and Pad Cells (input, output, Vdd pads). Location of all Standard Cells is automatically chosen by the tools during Placement based on routability and timing. Cells in a timing-critical path are placed close together to reduce routing-related delay. Routing along the timing-critical path is a priority for shorter and faster connection. Non-critical path are routed around critical areas to reduce routability problems for critical path and the timing does not impact by non-critical path. Place and Route is illustrated in Fig.7.

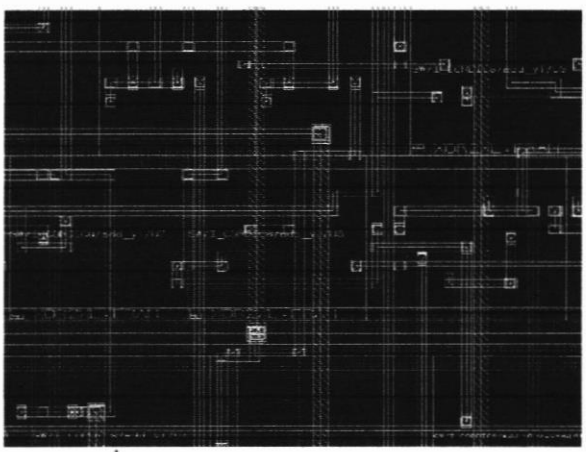

Fig.7: Place and Route (P&R)

D. *Design Rule Check (DRC), Layout vs Schematic (LVS).*

Design rule are a series of parameters provided by semiconductor manufacturer that enable the designer to verify the correctness of mask set. Design rule are

specific to a particular semiconductor manufacturing process where Silterra 0.18µm CMOS technology is used to perform this design. LVS is to ensure that the layout is correct realization of the intended circuit topology by comparing the layout and the RTL.

E. Static Timing Analysis (STA)

Static Timing Analysis is to perform while ignoring net C. The purposed is to verify the constrained netlist has good chance of meeting timing after Place and Route (P&R). The hole and setup time after performing STA is a positive value otherwise the layout need to be synthesis again.

F. Post-Layout Verification

Post-Layout Verification is to verify the layout and view the simulation of the layout. The existing testbench and other stimulus file are reused where the testbench play a big role in defining the result of the simulation. Insertion of IO buffer are perform after the core of the layout is verify.

IV. RESULTS AND DISCUSSION

The simulation result of SPWM using CORDIC is match between source code simulations using (ModelSim), RTL simulation (VirSim), and also layout simulation (VCS). The used of CORDIC is to provides an area-efficient architecture for effective design and the result prove that CORDIC able to reduce the size of the actual hardware of SPWM.

A. Comparing Simulations Result

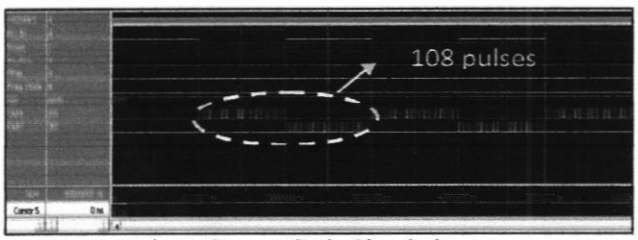

Fig.8: Source Code Simulation

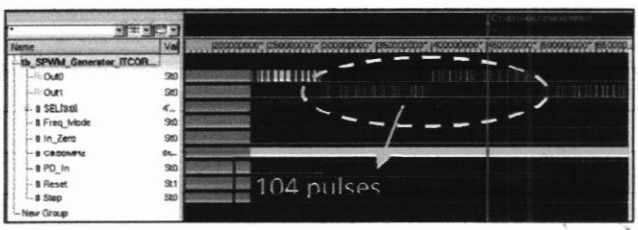

Fig.9: RTL Simulation

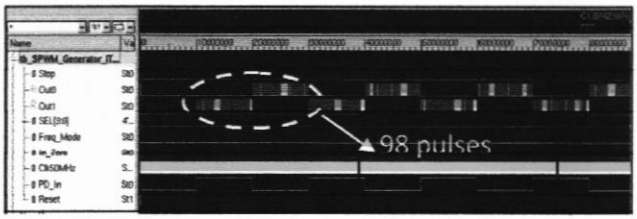

Fig.10: Layout Simulation

Figure above shows the simulations result for source code, RTL and also layout. From the simulation the result are tabulated below.

	Source Code	RTL	Layout
Number of pulse per cycle	108pulses	104pulses	98pulses

Table 1: Number of Pulse per cycle

Number of pulse width produced from this system can be calculated using equation (4). Thu number of pulse is ration from sine waveform frequency and triangle waveform frequency. For this system number of pulse (p) is 100 for 50Hz sine frequency waveform, (f_{ref}), and 5 kHz triangular frequency waveform, (f_c). Calculation for number of pulse per cycle:
The sine frequency waveform, (f_{ref}) is 50Hz, and 5 kHz triangular frequency waveform, (f_c).

$$\text{Sine frequency}, \quad f_{ref} = \frac{1}{T_{ref}} \tag{2}$$

$$\text{Triangular frequency}, \ f_c = \frac{1}{T_c} \tag{3}$$

$$\text{Pulse}, \ p = \frac{T_{ref}}{T_c} \tag{4}$$

T_{ref} = reffernce time
T_c = carrier time

The discussions that can be made by the result are in FPGA the frequency divider can't perform division of friction number, so the reference frequency (f_{ref}) that are sent is not exactly 50Hz. In RTL simulation, the pulse generated is 104 compare to 108 in the source code, this is because of the timing delay after the RTL is synthesis and also affected by the inaccurate of

reference frequency (f_{ref}). In layout design the pulse generated is only 98pulses per-cycle, this happen because the parasitic such as capacitance, lumped capacitance or RC coupling which will degrade performance of design and also course by the reference frequency (f_{ref}). Even the pulses that are generated are less compare to the source code result, the layout result still in the range of the specification.
The range of specification is between 90 to 110 bases on calculations that are made from front-end design. For this design, the worth case is taken as the operating point.

B. Effective Area

The size of core without IO buffer is 256µm X 260µm as shown in Fig.11. The total number of gate of this design is 2018 compare to the original design which is 4490 gates.

	Original Design (lookup table)	**New Design (CORDIC)**
Logic Element (gates)	4490	2018

Table 2: Comparison Logics Element

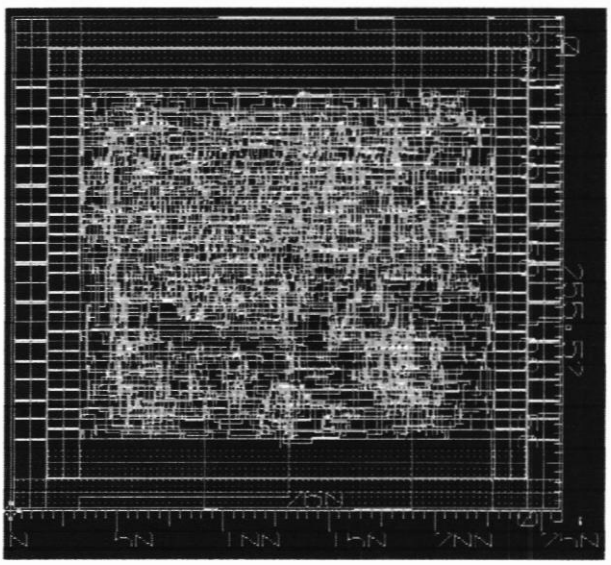

Fig.11: Core without IO buffer

The die size of the design is about 0.68mm X 0.68mm.The actual core with IO buffer are illustrated in Fig.12

	Core without IO buffer	**Core with IO buffer**
Area (mm)	0.26x0.26	0.68x0.68

Table 3: Effective Area based on CORDIC algorithm

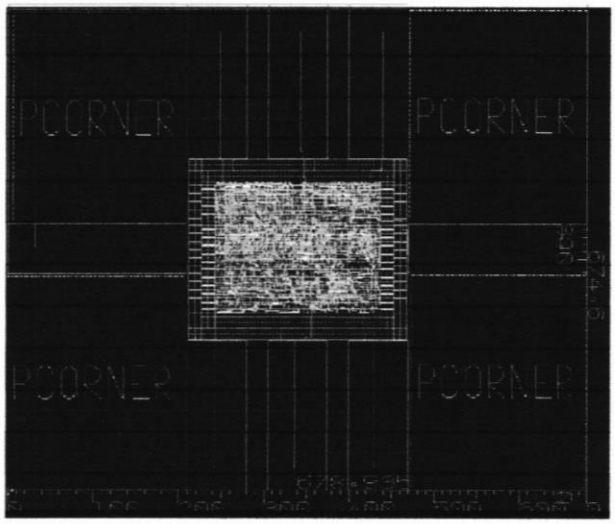

Fig.12: Core with IO buffer

V. CONCLUSION

It can be concluded that an area-efficient Sinusoidal Pulse Width Modulation (SPWM) has been designed using Verilog coding by representing the Coordinate Rotation Digital Computer (CORDIC) Algorithm to calculate trigonometric function performed by a shift and add operation instead by lookup table which is not an area-efficient. The approach in coding enables the design to be implemented in ASIC design such as Synopsys. In future this design is recommended to use a latest tool from Synopsys which is IC Compiler for more optimized and reduce the gate length to 120nm. . The design shall be tapeout for commercialization.

VI. REFERENCES

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