OPTIMIZATION OF GATE DIELECTRIC THICKNESS IN PMOS STRUCTURE USING SILVACO TCAD TOOLS

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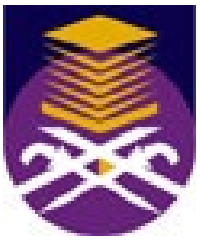

AYUB BIN BAKRI

FACULTY OF ELECTRICAL ENGINEERING

UNIVERSITI TEKNOLOGI MARA

40450 SHAH ALAM

SELANGOR, MALAYSIA

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ABSTRACT

The dielectric layer in Metal Oxide Semiconductor Field Effect transistor (MOSFET) is a layer of very thin oxide which serves as insulator between the gate and channel. It's also known as gate oxide or gate dielectric. This paper presents the effects of gate oxide thickness on p-channel MOSFET (PMOS) performance by optimizing the gate oxide thickness using Silvaco Technology Computer Aided Design (TCAD) software. The gate oxide thickness was found directly proportional to the threshold voltage. By using Silvaco TCAD, the optimum value obtained for gate oxide thickness is 3 nm. In the oxidation process the oxidation time is the best optimizer parameter compared to pressure and temperature. The optimum amount of HCl in oxidation process is 3%.

TABLE OF CONTENTS

CHAPTER 1

INTRODUCTION

1.1 INTRODUCTION OF PMOSFET

A MOSFET operates as a conducting semiconductor channel with two ohmic contacts, the source and the drain, where the number of charge carriers in the channel is controlled by a third contact, the gate. The gate contact is separated from the channel by an insulating silicon dioxide (SiO_2) layer. The charge carriers of the conducting channel constitute an inversion charge, that is, holes in the case of an n-type substrate (p-channel device), induced in the semiconductor at the silicon insulator interface by the voltage applied to the gate electrode [5]. The electrons enter and exit the channel at p+ contacts in the case of a PMOS. The basic structure of PMOS is shown in the figure 1.1 below.

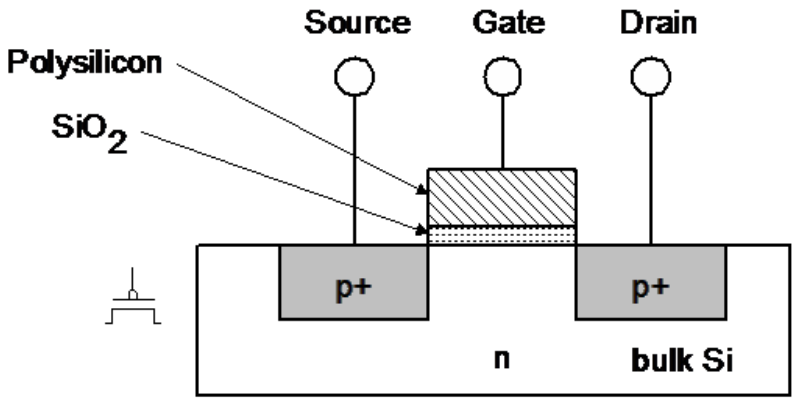

Figure 1.1: Basic structure of PMOS.

The flow of holes from the source to the drain is controlled by the voltage applied to the gate. A negative voltage applied to the gate, attracts holes to the interface between the gate dielectric and the semiconductor [5]. These holes form a conducting channel between the source and drain, called the inversion layer [5, 8].