THE DEVELOPMENT AND ANALYSIS OF THE STRAINED Si ON RELAXED $Si_{0.7}Ge_{0.3}$/Si N-MOS

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ABSTRACT

The electrical characteristics of the $Si_{0.7}Ge_{0.3}$ on relaxed Si N-MOS are compared with the conventional Si N-MOS developed by the simulation of basic fabrication processes. From the result, it will show that the $Si_{0.7}Ge_{0.3}$/Si N-MOS gives better performance than the Si N-MOS. Based on the simulated electrical characteristics, the strained SiGe/Si heterostructure influences the threshold voltage, Vt. From Id–Vg curve, the $Si_{0.7}Ge_{0.3}$/Si N-MOS has a 0.3V lower threshold voltage compare to conventional Si N-MOS means that reduction until 46.15% of Vt occur. The faster turn on of transistor is important to achieve a high speed in complementary MOS technology.

The $Si_{0.7}Ge_{0.3}$/Si N-MOS are also developed in three n-channel lengths that are 1.2 μm, 1.0 μm and 0.8 μm. The decreased of n-channel length will increase the saturated current. The term of low Vt and higher Id saturation as shown in Id-Vd curves means less power supply and faster to turn on. The threshold voltage of $Si_{0.7}Ge_{0.3}$/Si N-MOS can be reduced until 55.96% from conventional Si N-MOS and the figure keep regress when decreases the channel length.

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CHAPTER 1

INTRODUCTION

1.1 Overview

The metal-oxide-semiconductor field-effect transistor (MOSFET or MOS-FET) is by far the most common field-effect transistor in both digital and analog circuits. The MOSFET is composed of a channel of n-type or p-type semiconductor material and is accordingly called an N-MOSFET or a P-MOSFET [6].

The basic structure of n-channel MOSFET consist of four terminal devices that are p-type substrate, in which two n^+ diffusion regions, the drain and the source. The surface of the substrate region between the drain and the source is covered with a thin oxide layer and metal or polysilicon gate is deposited on top of this gate dielectric. The two n^+ regions will be the current conducting terminals of the device. The device structure is completely symmetrical with respect to the drain and sources region. The different roles of these two regions will define in conjunction with the applied terminal voltages and the direction of the current flow [5].

A conducting channel will eventually be formed through applied gate voltage in the section of the device between the drain and source diffusion region. The distance between the drain and source diffusion regions is called the channel length (L) as in figure 1.1 and the lateral extent of the channel (perpendicular to the length) is the channel width (W). The channel length, the channel width and the thickness of the oxide layer covering the channel region are important parameters which can be used to control some of the electrical properties of the MOSFET [5].