CORRELATION STUDY OF DOUBLE STACK DIELECTRIC MOS CAPACITOR SIMULATION MODEL WITH FABRICATED SAMPLE USING TCAD SILVACO

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ABSTRACT

Capacitance voltage measurements of MOS capacitor structure provide a wealth of information about the structure which is of direct interest when one evaluates an MOS process. This research paper discussed about the correlation study of simulation model for double stack dielectric MOS capacitor with the fabricated industry standard sample from wafer FAB. The SILVACO Athena and Atlas simulator software have been used for the analysis study. It should accurately describe and model the process parameters. This model could be used for process optimization in simulation mode then helps to reduce the process optimization time and the experiment cost which normally require many round of experiment in clean room. Capacitance model of MOS capacitor are directly related to its physical parameters. Therefore, the capacitance-voltage (C-V) characteristics of MOS capacitor were used as a diagnostic tool in this study to correlate the physical parameter and its capacitance value. Varying the dielectric thickness, dielectric permittivity and the size of MOS capacitor have been considered in the simulation to correlate the simulation output and measured value on the fabricated sample. A closed correlation between simulated and measured sample were published in this paper.

Index Terms – MOS Capacitor, C-V characteristics, Dielectric Thickness, Dielectric Permittivity, Size of MOS capacitor, SILVACO Athena and Atlas Simulator.

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CHAPTER 1

INTRODUCTION

1.1 BACKGROUND

The major part of MOS technology is the metal – oxide – semiconductor (MOS) structure. When this structure, commonly referred as MOS capacitor, is connected as a two terminal device, with one electrode connected to the metal and the other electrode connected to the semiconductor, a voltage dependent capacitance results [1]. The ideal MOS capacitor structure is quite similar with the MOSFET except there are no source/drain regions. It was introduced long time ago in late 1950s when Dawon Kahng and Martin M. (John) Atalla from Bell Labs invented the metal–oxide–semiconductor field-effect transistor (MOSFET). Nowadays, MOS Capacitor is still relevant and widely used in many applications. The fabrication of this type of device require high standard of clean room environment in order to produce high quality of fabrication process. High quality of dielectric layers should be used for MOS capacitor to ensure there is no leakage issue on the gate and to keep the breakdown voltage high. This requires a very good control of process fabrication. It's however leads to high production cost using expensive equipment and time consuming. But for study purposes in order to guide real experiment in clean room and process optimization, simulations software are normally used. One of the simulation tools for wafer fabrication is ATHENA and ATLAS modules of TCAD SILVACO software. These tools can help engineers to study the process capability as well as the process effects to the device performances. In real process fabrication however, there are always some process variations that affect the device performance. In this research, correlation study between process variations and the device parameters have been done.