LOGICAL EFFORT USING PARTICLE SWARM OPTIMIZATION ALGORITHM – AN EXAMINATION ON THE 8-STAGE FULL ADDER CIRCUIT

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Sincerely,

Muhammad Aiman bin Johari

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INTRODUCTION

1.1 Problem Statement

In semiconductor manufacturing, the fabrication cost of integrated circuits (I.C's) are associated with the development time and the materials used (chip area), where it can affect the speed and power requirements. Before choosing the best design, the goodness of each option, especially regarding the speed and power consumption must be determined. The speed and power consumption in the digital circuits depends on the gate sizing of that circuit which means that the best gate sizing will give the efficient speed and the low power consumption to that circuit.

The method of Logical Effort (LE) has recently been introduced to allow for both quick and accurate analysis of Complementary Metal Oxide Semiconductor (CMOS) circuits. But, the limitation of the LE method (such as time spent to calculate the delay and also try and error method to find the specific delay) must be avoided to reduce the cost. By applying Particle Swarm Optimization (PSO) method, the LE problem for electronic circuits is solved automatically, to find the gate sizing within a short period of time. The best gate sizing that will be determined will give the required delay, where it is the best choice for certain applications such as in embedded computers.

A PSO algorithm has been proposed for the LE problems to find the delay and best gate sizing. This method is applied to the Full Adder (FA) logic gate circuit, a very basic and slow digital arithmetic design but may be the best choice for certain applications such as embedded computers where circuit delay is a key requirement. The scope of this project is to apply the PSO algorithm to solve the LE problem. The idea of operation is similar to the LE method, but the PSO method was used to modify the size of the gates. To achieve this idea, first, the theory of LE must be studied first because it is important before the minimum possible delay can be estimated. Then, the LE problem for