4 BIT FULL ADDER LAYOUT AND ANALYSIS USING LASI AND WINSPICE

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ABSTRACT

This paper presents a project on the designing the 4 bit full adder layout using LASI software. Design parameters in this project are 5V supply voltage, the technology is 1.0μm from LASI software and also the 2μchip library from LASI software is used. In this project, the tasks are divided into 3 phases. Phase 1 is the construction of each logic gate using the cells that are already in the library in the LASI software. The standard cells in the library are INVERTER, NAND and NOR gate. Phase 2 is the completion of 4 bit full adder by combining each cells in phase 1 by manually connected or used the auto placement & route in LASI 7. Finally, phase 3 is the extraction of the t_{rise}, t_{fall} and total capacitance.

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CHAPTER 1

INTRODUCTION

1.0 Introduction

In this project, a 4-bit full adder layout is designed using LASI software. First, an individual of a hierarchical layout of a half adder, full adder and 4 bit adder using LASI is drawn. Then the layouts are simulated using SPICE to confirm that each design is working.

The hierarchical Layout design is done using Lasi.N3X2, P3X2. The basic gates such as NAND, XOR, Half-Adder, Full-Adder and 4 bit Full Adder layouts are made in hierarchical fashion using bottom up approach. To analyze each cell, Winspice3 .CIR file is used created by LASI.

Design parameters for this project are:

Supply voltage	: 5V
Technology	:1.0 um (2uchip)
Simulation	: Win SPICE
Library	:2uchip (import the standard cells)