IMPLEMENTING FREQUENCY TRANSLATION BY ADAPTING DIGITAL PHASE SHIFTER FOR WCDMA USING XILINX

Thesis submitted to the Faculty of Electrical Engineering, Universiti Teknologi MARA in fulfillment of the requirement for the Degree of Bachelor of Engineering

MOHD KHALILI BIN ZAKARIA
FACULTY OF ELECTRICAL ENGINEERING
UNIVERSITI TEKNOLOGI MARA
40450 SHAH ALAM
SELANGOR DARUL EHSAN

NOVEMBER 2009

ACKNOWLEDGEMENT

In the name of Allah, the most Beneficent and Merciful, with the deepest gratefulness to Allah who has given me this full of strength in order to complete this thesis.

First and foresmost, I would like to express my gratitude to my project supervisor Mrs. Norhazlin for her assistance and guidance. Not to be forgotten to Mr. Abdul Hadi who has helping me understanding the project since the beginning.

Furthermore, with the brilliant idea given from Dr Azilah Saparon and Miss Harnani also were meant so much to me along the way to fulfill this project.

Herein, I would like to emphasize this thankfulness to my family members especially my parents Zakaria bin Abdul Manan and for their advices, prayer, encouragement and continuous moral supports for the completion of my study in UiTM.

Last but not least, I would like to dedicate this thankfulness to my friends, lecturers, staff and supporting staffs especially Nik Azman who has been helping me a lot during finishing this project in various ways.

Mohd Khalili bin Zakaria

Bachelor in Electrical Engineering (Hons.)

Faculty of Electrical Engineering

Universiti Teknologi MARA

Shah Alam, Selangor

ABSTRACT

This thesis is to perform phase shifting of sampled digitized frequency in signal that is using Phase Lock Loop (PLL) undersampling conversion in WCDMA. Shifting of the digital data is very important as to make sure that the translated data is shifted correctly into register so that no missing the data. The detail design of frequency translation will be focusing on the digital phase shifter, where it is usually comprised in direct digital synthesizer (DDS) which then utilizes every digitized waveform signals stored in the register. The digitized signals will then shifted according to the designed algorithm so that every data will follows its sequence and shifted as desired. Algorithm of the design will be written in VHDL programming Language which then simulated through Modelsim SE 6.3f. The sequence data shifted can be seen by simulating the written program of its test bench by mapping the entire written block diagram based on the algorithm. XILINX ISE simulator is used to synthesize the block diagram of the digital phase shifter design utilization.

TABLE OF CONTENT

CHAPTER 1

INTRODUCTION

This thesis will explain about the design of the Digital Phase Shifter that will be implemented in the WCDMA system. The system is comprised of Digital Signal Processor (DSP), Direct Digital Synthesizer (DDS), Frequency Translation and also the Digital Phase Shifter that will be explained later.

1.1 Problem Statements

Frequency translator comprised of fast switching digital phase shifters. The input binary advances of retards the phase in discreet increments. The device is switched periodically through 360 degrees in increments that are equal to the LSB. The frequency translator converts the frequency of RF carrier to lower or higher frequency.

The significant of the project is that the shifting algorithm that is used will provide proper data shifting at its specific angle of the digital phase shifter. Which then to be used as a frequency translation that can be applied for the DSP of the WCDMA system

1.2 Objectives of Work

The purpose of this project is to study the fundamental theory of Digital Phase Shifter and how it can be designed and implemented by using Xilinx's FPGA. It is very crucial to understand the shifting algorithm of the Digital Phase Shifter within how its work according to the necessary specifications. Furthermore, it is very important to be able to design the programming instruction needed for the data shifting capability. Not to be lack of as to provide the proper shifting of each sampled data so that it is shifted according to its sequence and register allocation. The work include the digital phase shifter design analysis and simulation using Modelsim and Xilinx Synthesis tool. The digital phase shifter design includes the RAM memory, Register, ROM instruction, Arithmetic Logic Unit (ALU), Controller, Program Counter (PC) and microcontroller (uC) for the mapping