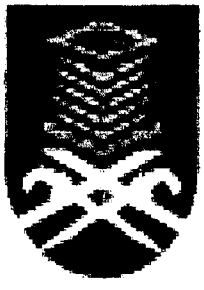
DESIGN BUILT-IN SELF-TEST FOR CONTROL SEQUENCER CIRCUIT USING XILINX

This project presented as a fulfillment for the award of the
Bachelor in Electrical Engineering (Hons)
Of
UNIVERSITI TEKNOLOGI MARA



NURUL AINI BINTI MOHAMED ISA
Faculty of Electrical Engineering
UNIVERSITI TEKNOLOGI MARA
40450 SHAH ALAM, SELANGOR
MALAYSIA

ACKNOWLEDGEMENT

All praises be to Allah, Lord of Universe , the Merciful and Beneficent Salam to Nabi Muhammad s.a.w, his friends, companion and the people who follow this path. Alhamdulillah for giving the me a good health and patience for completing this thesis and also my study.

I would like to express my deepest thanks to my supervisor Professor Madya Kartini Salam for her kindness, support and concern of my Final Year Degree Project (KJE 554). Also my special appreciation to Encik Muhammad Nazir Mohd Khalid for his times and valuable information towards the accomplishment of this project.

I am also indebted to the various help and discussions offered by fellow friends and their giving ideas , support and providing access materials for the completion for this project.

Finally, I would like to thanks my family especially my father Haji Mohamed Isa Mahamood and my mother for their patience, support and continuing encouragement.

Thank you.

Nurul Aini Mohamed Isa
Faculty of Electrical Engineering
UNIVERSITI TEKNOLOGI MARA
Shah Alam, Selangor Darul Ehsan

March 2004

ABSTRACT

An alternative to applying test vectors from an external tester is a built-in self-test (BIST). The development of BIST based on determined test pattern generation (random pattern generation) using LFSR. BIST strategies use pseudo-random sequences as the test sequences. In part of the design process BIST require extra pin which become from three ports such as sequencer circuit (CUT), Test Pattern Generation (TPG) and Linear Feedback Shift Register (LFSR).

The sequencer circuit is a circuit that displayed the outputs of sequences number. It was chosen as a sample of IC subsystem due to its widely used in most Digital-Signal-processing (DSP) chip. Sequencing is an assembly term refers to arranging axial/radial components in their order of insertion sequence, and to prepare new tape/reel by a sequencer.

Among the different approaches to testing ICs, the use of pseudo-random vectors in self-testing has been employed efficiently, where linear feedback shift register (LFSR) are commonly used as the pseudo-random vector generator. It can generate the value of an input of the circuit.

For the Test Pattern Generation, sequencer circuit is chosen as CUT that allowed applying deterministic technique in order to find the entire possible fault in the circuit.

Outputs of sequencer number are showed by Signal Analyzer. Comparator is chosen to compare whether the CUT is faulty or fault-free.

TABLE OF CONTENTS

CHAPTER 1

INTRODUCTION

1.1 Background

Testing of integrated circuits (ICs) is of crucial importance to ensure a high level of quality in product functionality in both commercially and privately produced products. The impact of testing affects areas of manufacturing as well as those involved in design. Given this range of design involvement, how to go about best achieving a high level of confidence in IC operation is a major concern. This desire to attain a high quality level must be tempered with the cost and time involved in this process. These two design considerations are at constant odds. It is with both goals in mind (effectiveness vs. cost/time) that Built-In Self-Test (BIST) has become a major design consideration in Design-For-Testability (DFT) methods.

BIST is beneficial in many ways. First, it can reduce dependency on external Automatic Test Equipment (ATE). This aspect impacts the cost/time constraint because the ATE will be utilized less by the current design and can be used elsewhere or on other devices. In addition, BIST can provide at speed, in system testing of the Circuit-Under-Test (CUT). This is crucial to the quality component of testing. In addition, BIST can overcome pin limitations due to packaging, make efficient use of available extra chip area, and provide more detailed information about the faults present. All these benefits are plentiful motivations for BIST [1].

In the early 1990s , the use of Automatic Test Pattern Generation (ATPG) programs became popular to generate manufacturing tests for VLSI designs. Soon the test circuitry must be added to a design to simplify ATPG. It is now possible to efficiently fabricate ICs with several million gates due to the rapid advances in semiconductor manufacturing technology. The increased size and complexity of System-on-Chip (SOC) designs have, however, reduced the effectiveness of