A STUDY ON EFFECT OF N-WELL TO THE THRESHOLD VOLTAGE IN 65 nm NMOS STRUCTURE

Ahmad Luqman Bin Mohammed Shaihani
Faculty of Electrical Engineering
Universiti Teknologi MARA
40450 Shah Alam, Malaysia
luqman_cimb@yahoo.com

Abstract *– A study on effect of N-well to the threshold voltage in 65 nm NMOS structure was conducted. The N-well in this paper refers to source and drain regions. Few parameters including concentration and energy that effect source and drain implantation have been altered using impurity of phosphorus. For annealing process, several parameters presented also were varied to get the optimum value of threshold voltage (Vth) that was 0.182929V which approximately closed to the recommended guideline from ITRS. All simulations were done by using SILVACO.*

Keywords: 65 nm NMOS, Threshold Voltage (Vth), Source and Drain(S/D).

1.0 INTRODUCTION

The entire semiconductor industry is heavily reliant on one device which is the MOS transistor as shown Figure 1. In other words, the industry is focusing on making circuits with MOS transistors and shrinking the circuit feature sizes so as to give more powerful and faster circuits with lower cost. In fact, one of the hallmarks of the semiconductor industry is the continuous scaling of circuit dimensions with the introduction of every new technology generation [4]. However, as the scaling of the MOS transistor comes to the submicron range (0.1um to below), many unexpected problems occurred [1].

There are two types of MOS transistor, the NMOS and PMOS. In the case of an NMOS device, the source and drain are commonly phosphorus-doped (n-type, rich in electrons) on the p-type substrate (rich in hole). In order, to fabricate the 65nm NMOS device, the gate length must be equal to 65nm and impurity type of substrate is p-type. At this size 65nm of MOS, one of the difficulty to set the fabrication recipe because of the non-linearity of the physicals and electrical characteristics [1].

The scaling of NMOS device to submicron range must have increasingly thinner gate dielectrics and lower threshold voltages for high-speed application [2]. Because of that, threshold voltage (Vth) is one of the most important NMOS device parameter. This is defined by the voltage on which drain current begins to flow through the channel of the transistor at an ON state. At the usual bulk NMOS; this voltage is controlled by introduction of the impurities into a silicon substrate. Threshold voltage, value can be affected by many factors such as polysilicon type, gate oxide thickness, concentration under the gate and the source and drain (active area). Each factor contribute to different value to threshold voltage, however the source and drain gives a major effect to the threshold voltage value [1]. The result from each parameter in source and drain implant and anneal were analyzed and conclusions were made. The International Technology Roadmap for Semiconductor (ITRS) states that the value of threshold voltage, Vth should be 0.18V±12.7% is being used as the guideline for 65nm NMOS structure to achieve the objective of this research [6].

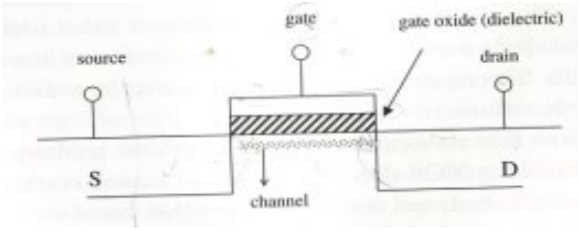

Figure 1: An MOS transistor

2.0 METHODOLOGY

Computer simulation is now an essential tool for research and development of semiconductor process and device. Costs can be dramatically reduced by using simulation instead of experimentation, as much as possible, to fine-tune the process recipe [5].

SILVACO TCAD TOOLS needed by two; ATHENA Process Simulation Frame work and ATLAS Device Simulation Software. ATHENA is a framework program that integrates several smaller

programs into a more complete process simulation tool. This program's focus is upon the simulation of fabrication processes as shown Figure 2. Another Silvaco Tcad tools been used was the ATLAS Device simulation software. Device can be created in ATLAS through layout based simulation syntax however the main focus of this program is simulation of the device once fabrication is completed.

- Mesh Grid
- Define Initial Substrate P-Type
- Grow Gate Oxide 20Angstrom
- Adjust VTH Implantation Using Bf2
- Gate Polysilicon Formation
- Polysilicon Doping And Ldd
- Spacer Formation Using Oxide
- S/D Implantation And Annealing
- Metallization Formation

Figure 2: Fabrication Process

After completing the 65nm NMOS structure process, the value of threshold voltage and Id vs Vgs curve was obtained by using ATLAS. For the threshold voltage, drain source voltage (Vds) is set to 0.1V. Five different parameters were used to study the effect of source and drain in the threshold voltage. Besides that, each parameter was altered with four different parameter values. When one parameter was altered, the other parameters were fixed at certain value. In this experiment, the fixed value for concentration at 4e13 ions/cm^2, energy at 10 KeV, temperature 900 ^{0}C, pressure at 1 Atm and time at 1 minute. Each parameter value was analyzed and conclusions were made to choose the best value for each parameter. Firstly, concentration of phosphorus from 3e13 ions/cm^2 to 6e13 ions/cm^2 was altered. Each level concentration was given a different value of threshold voltage even though the increasing concentration is in a small value. Next, the energy was altered from 9 KeV to 12 KeV at source and drain implant. After that, the experiment continues with the parameter source and drain annealing with altered factors such as temperature, pressure and time. Firstly, temperatures were altered at level 895 ^{0}C to 910 ^{0}C. Then, the pressure was altered from 1 Atm to 100 Atm. Finally, the time annealing was altered at 0.5 minutes to 2 minutes. Each parameter in source and drain implant and anneal results in different value of threshold voltage. All the process source and drain implant and anneal were summarized in flow chart at Figure 3.

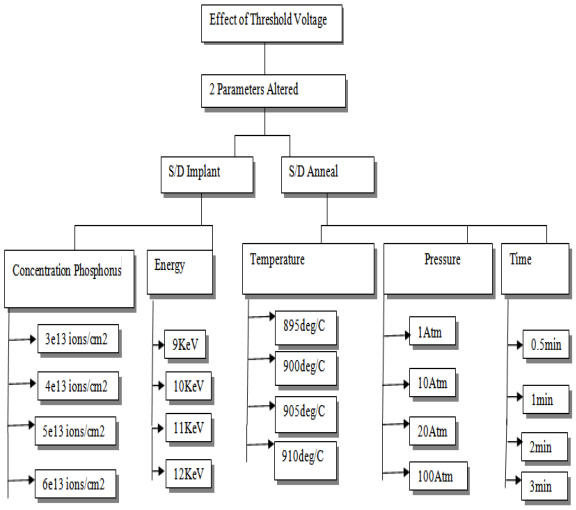

Figure 3: Flow Chart of Source/Drain(S/D) Implant and Anneal Parameters Altered.

3.0 RESULTS AND DISCUSSIONS

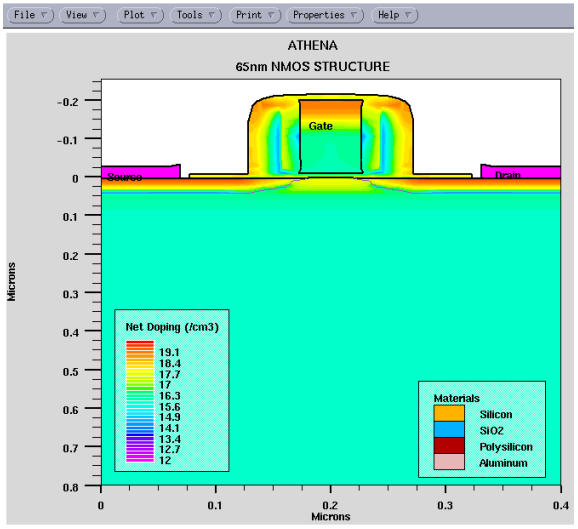

Figure 4: A 65nm NMOS Structure.

Figure 4 shows the final structure of 65 nm NMOS after completing all the fabrication processes in ATHENA mode.

Five different parameters were used to study the effect of source and drain in the threshold voltage for in each case.

Case 1: Altered concentration of phosphorus from 3e13 ions/cm^2 to 6e13 ions/cm^2 . Energy was fixed at 10 KeV, Temperature at 900 ^{0}C, Pressure at 1 Atm and Time at 1 minute.

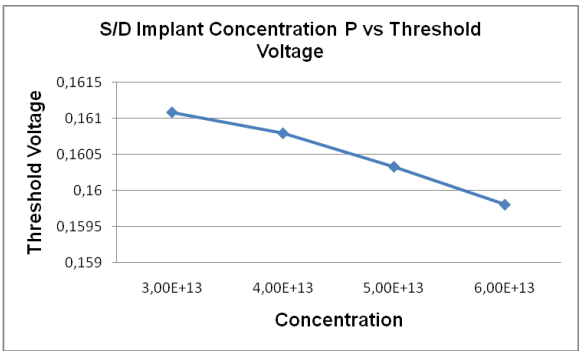

Figure 5: S/D Implant Concentration Phosphorus vs Threshold Voltage

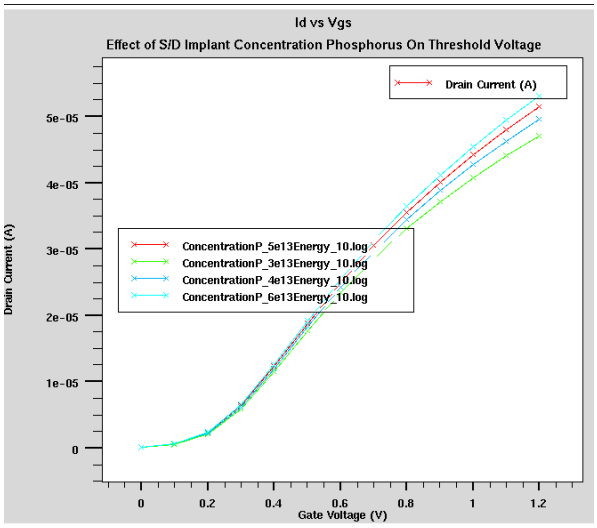

Figure 6: Id vs Vgs [Effect of S/D Implant Concentration Phosphorus on Threshold Voltage].

From Figure 5, the threshold voltage depends on the concentration of phosphorus because when the concentration of phosphorus increases, the threshold voltage will decrease. This reduction in threshold voltage (Vth) due to the number of electron in source and drain increases as concentrations implant increases. The optimum value of concentration was 3e13 ions/cm^2 and the threshold voltage value was 0.161079 V. The result from different threshold voltage is shown by Figure 6 in ATLAS mode.

Case 2: Fixed concentration of phosphorus at 4e13 ions/cm^2, Temperature at 900^{o}C, Pressure at 1 Atm and time at 1 minute. Energy was altered at 9 KeV to 12 KeV.

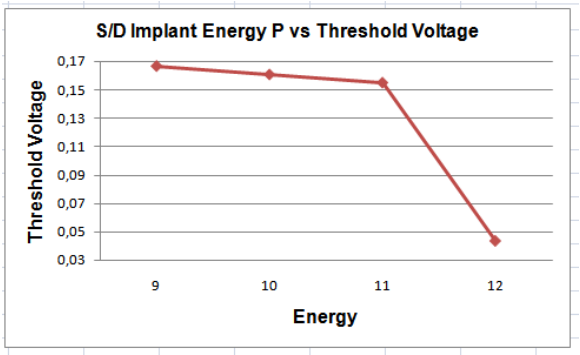

Figure 7: S/D Implant Energy Phosphorus vs Threshold Voltage

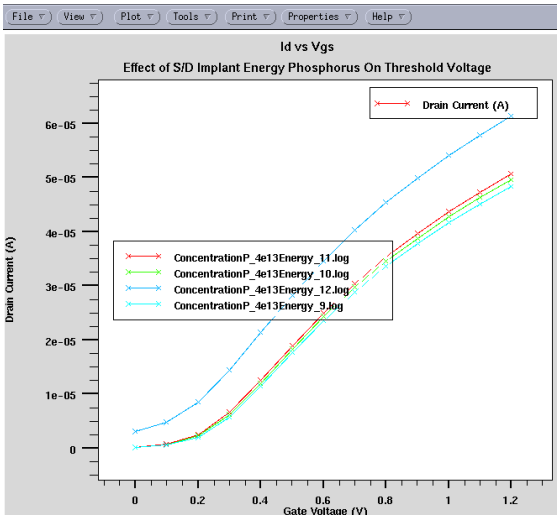

Figure 8 : Id vs Vgs [Effect of S/D Implant Energy Phosphorus on Threhold Voltage]

As shown in Figure 7 with an increase in energy, the value of threshold voltage decreases due the energy of the implantation increase as the ion will get more energy to go further into the silicon. Thus, the area of source and drain getting larger and the length between source and drain become narrower. Moreover, the threshold voltage also decreases since the electric field required is less to create the n-channel. Referring to the Figure 8, the threshold voltage dependence on the energy was shown. The best value of energy was 9 KeV where the threshold voltage obtained was 0.166759 V. The results obtained explained by the Figure 8 that show the different of threshold voltage.

Case 3: The temperature was varied from 895 ^{0}C to 910 ^{0}C. Time was fixed at 1 minute, pressure at 1 Atm, concentration at 4e13 ions/cm^2 and energy at 10 KeV.

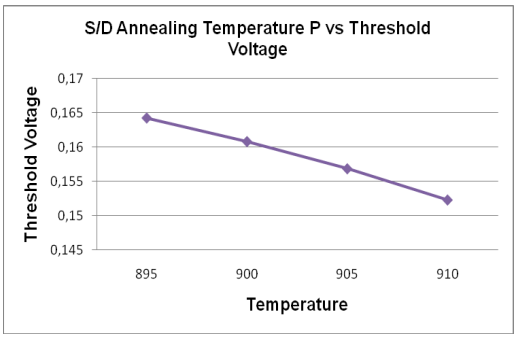

Figure 9: S/D Annealing Temperature Phosphorus vs Threshold Voltage.

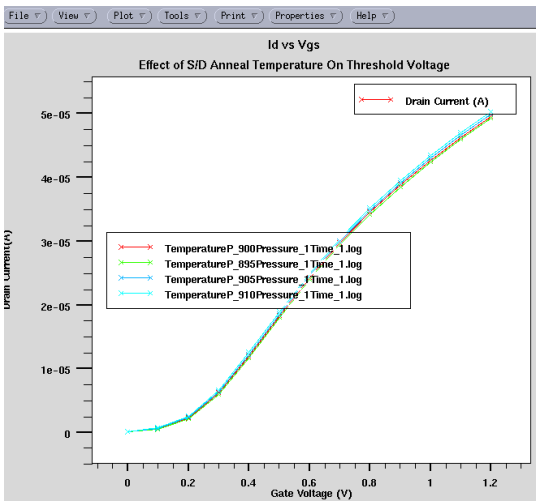

Figure 10: Id vs Vgs [Effect of S/D Anneal Temperature On Threshold Voltage].

When the temperature increased, the values of threshold voltage were reduced. As a result, threshold voltage is dependant on temperature as shown Figure 9. In fact, the concept of temperature is same as energy, because when the temperature increase, the electron go deep to the substrate diffuse from high concentration to the low concentration. In this case, when the value temperature was at 895 ^{0}C the threshold voltage obtained was 0.164224 V. The result obtained was pictured by the log of Figure 10 of ATLAS mode with different threshold voltage.

Case 4: Altered the pressure from 1Atm to 100 Atm. The value of time was fixed 1 minute, temperature at 900 ^{0}C, concentration at 4e13 ions/cm^2 and energy at 10 KeV.

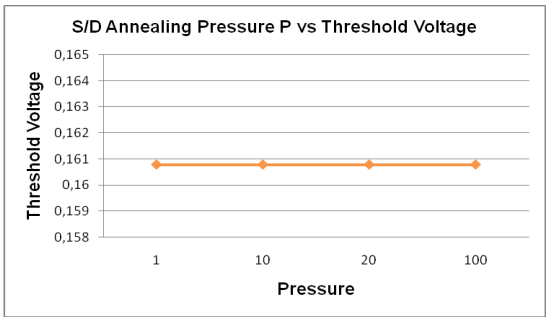

Figure 11: S/D Annealing Pressure Phosphorus vs Threshold Voltage

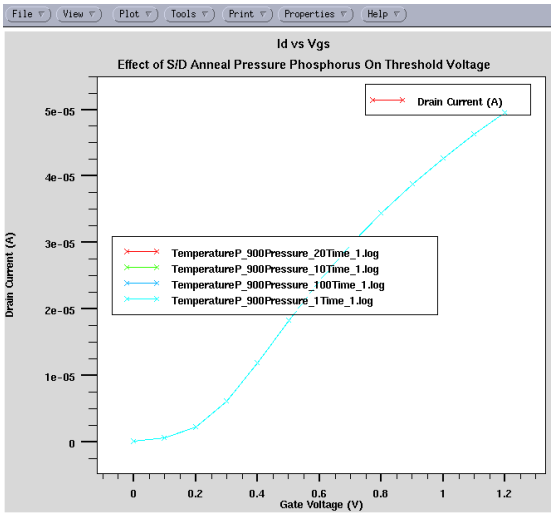

Figure 12: Id vs Vgs [Effect of S/D Anneal Pressure On Threshold Voltage].

In the source and drain annealing, the pressure was not influenced by the temperatue. Therefore, threshold voltage was not affected when the pressure increased as shown Figure 11. The suitable pressure at 1 Atm were chosen in order to obtain threshold voltage at 0.160789V. The result of same threshold voltage at Id vs Vgs curves is shown Figure 12.

Case 5: Altered the time from 0.5 minutes to 3 minutes. The value of pressure was fixed at 1 Atm, temperature at 900 ^{0}C, concentration at 4e13 ions/cm^2 and Energy at 10 KeV.

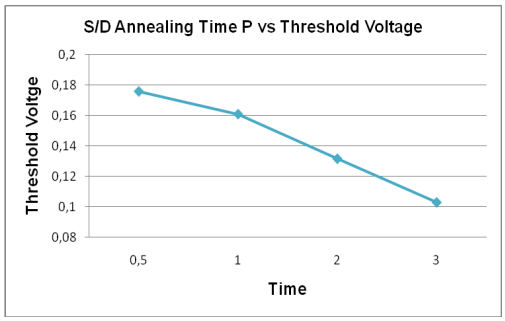

Figure 13: S/D Annealing Time Phosphorus vs Threshold Voltage

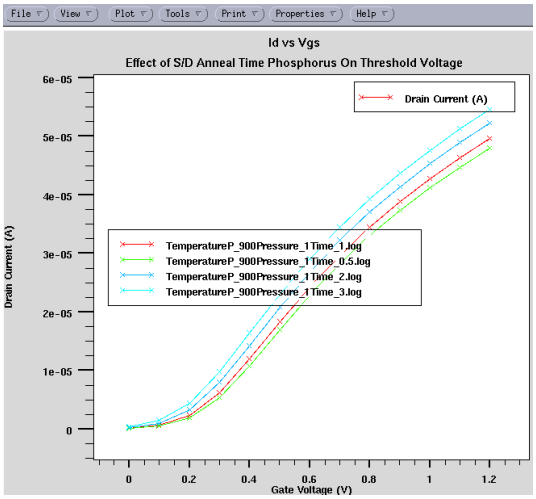

Figure 14: Id vs Vgs [Effect of S/D Anneal Time On Threshold Voltage].

Time for annealling process are very important during the source and drain annealing. In addittion, temperature depends on time. In other words, threshold voltage depends on time as shown in Figure 13. The longer time is taken, the deeper the electron will go to substrate and diffuse from high concentration to the low concentration where the n-channel formation become smaller thus reducing gate voltage. In this case, the time for annealing was 0.5 minute and the threshold voltage was 0.175654 V and was considered the best value. The different threshold voltage and shown by the Figure 14 for ATLAS mode.

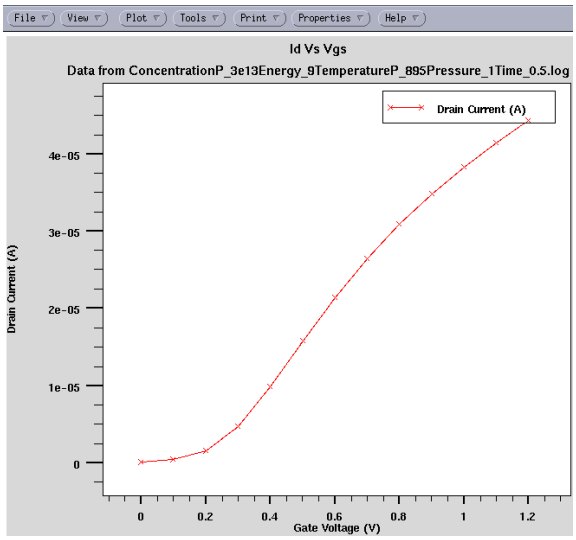

Figure 15: Id vs Vgs Curve.

4.0 CONCLUSION

Each parameter in source and drain results in different value of threshold voltage. Five different parameters were varied to study the effect of source and drain in the threshold voltage. Therefore, each parameter in source and drain implant and anneal was altered such as the concentration of phosphorus, energy, temperature, pressure and time. The best threshold voltage obtained was 0.182929 V as shown in Table 1 and pictured in Figure 15 for Id vs Vgs curve which was obtained in ATLAS mode that is approximately closed to the guideline recommended by ITRS.

Table 1: The Optimum Parameter Value at Source and Drain (S/D).

Concentration Impurity of Phosphorus	3e13 ions/cm^2
Energy	9 KeV
Temperature	895^{0}C
Pressure	1 Atm
Time	0.5 minutes
Threshold voltage	0.182929 V
Recommended Threshold Voltage by ITRS	0.18V±12.7%

5.0 FUTURE RECOMMENDATION

Threshold voltage can be affected by many factors such as polysilicon type, gate oxide thickness, concentration under the gate and active area (source and drain). This research has greater opportunity to be fabricated to nanoscale device concerning the threshold voltage of device. This process can be integrated with halo implantation in order to achieve the precise threshold voltage especially device with shallow junction since the stability of threshold voltage is very crucial for the nanoscale device [3].

6.0 ACKNOWLEDGMENT

Alhamdullillah, it is only with Allah's will that the author was able to complete this project. The author wants to thank his supervisor, Miss Rafidah Rosman and also to his co-supervisor PM Dr Mohamad Rusop Bin Mahmud for their guidance, opinion and suggestion upon completing this project. The unconditional love my parents showed me strengthened my resolve in doing this project and doing it to the best of my abilities. The author would also like to thank my classmates for being a vast reservoir of assistance. All in all, Alhamdullillah and may Allah bless us all.

7.0 REFERENCES

1] T. Z. Mohamad, Ibrahim Ahmad, Azami Zaharim, "Optimum solution in fabricating 65 nm NMOS transistors using Taguchi Method," Faculty of Engineering, Universiti Kebangsaan Malaysia.

2] M.R. Mirabedini, V.P.Gopinath, A.Kamath, M.Y.Lee, and W.C.Yeh"65nm Transistor for 90nm CMOS SOC Platform", Process and Technology Development, LSI Logic Corporation, Santa Clara, CA 95054, USA.

3] H.Hwang, D.H. Lee, J.G.Ahn, J. S.Byun, and D.Yang "Effect of channeling of halo implantation on threshold voltage shift of MOSFET," Advanced Technology Department, ULSi Laboratory, Lg Semicon Co, Ltd, 1Hyangjeong-dong, Humgduk-gu, Cheongju 350-480, Korea.

4] "The National Technology Roadmap for Semiconductors: Technology Needs," Semiconductor Industry Association, San Jose, Calif.1997.

5] Harish B.P."Process Simulation for 65nm" Micoelectronics Lab, Dept. of Electrical Commmunication Engg.,Indian Institute of Science, Bangalore.

6] Semiconductor Industry Association, The International Technology Roadmap for Semiconductors, 2004 edition.