A STUDY ON EFFECT OF N-WELL TO THE THRESHOLD VOLTAGE IN 65nm NMOS STRUCTURE

This project report is presented in partial fulfillment for the award of the

Bachelor in Electrical Engineering (Hons.)

Of

UNIVERSITI TEKNOLOGI MARA (UiTM)

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ACKNOWLEDGEMENT

In the name of ALLAH, Most Generous and Most Merciful.

It is with the deepest sense of gratitude of the Almighty ALLAH who gives strength and ability to complete this thesis project. All good aspirations, devotions and prayers are due to ALLAH whose blessing and guidance have helped me throughout to entire project.

I would like to take this opportunity to express my appreciation to my supervisor, Miss Rafidah Rosman and also to my co-supervisor PM Dr. Mohamad Rusop Bin Mahmud for guiding me and sharing with me his knowledge and experience in order to complete this project. Her guidance, advice, co-operation, encouragement and useful ideas were very much appreciated.

To unconditional love my parents, sisters and brother, deepest thank you for your pray and always being supportive in whatever I have done. My sincere thank also goes to all my friends including everyone who helped me directly and indirectly in completing this project. All in all, Alhamdullillah and may Allah bless us all.

ABSTRACT

A study on effect of N-well to the threshold voltage in 65 nm NMOS structure was conducted. The N-well in this research refers to source and drain regions. Few parameters including concentration and energy that effect source and drain implantation have been altered using impurity of phosphorus. For annealing process, several parameters such as temperature, pressure and time presented also were varied to get the optimum value of threshold voltage (Vth) that was 0.182929V which approximately closed to the recommended guideline from the International Technology Roadmap for Semiconductor, (ITRS). All simulations were done by using SILVACO TCAD TOOL software. ATHENA and ATLAS module of SILVACO software are tools used in simulating the fabrication process and simulating the electrical performance of 65 nm NMOS structure.

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CHAPTER 1

INTRODUCTION

1.1 BACKGROUND OF STUDY

The entire semiconductor industry is heavily reliant on one device which is the MOS transistor as shown Figure 1. In other words, the industry is focusing on making circuits with MOS transistors and shrinking the circuit feature sizes so as to give more powerful and faster circuits with lower cost. In fact, one of the hallmarks of the semiconductor industry is the continuous scaling of circuit dimensions with the introduction of every new technology generation [4]. However, as the scaling of the MOS transistor comes to the submicron range (0.1um to below), many unexpected problems occurred [1].

There are two types of MOS transistor, the NMOS and PMOS. In the case of an NMOS device, the source and drain are commonly phosphorus-doped (n-type, rich in electrons) on the p-type substrate (rich in hole). In order, to fabricate the 65nm NMOS device, the gate length must be equal to 65nm and impurity type of substrate is p-type. At this size 65nm of MOS, one of the difficulty to set the fabrication recipe because of the non-linearity of the physicals and electrical characteristics [1].

The scaling of NMOS device to submicron range must have increasingly thinner gate dielectrics and lower threshold voltages for high-speed application [2]. Because of that, threshold voltage (Vth) is one of the most important NMOS device parameter. This is defined by the voltage on which drain current begins to flow through the channel of the transistor at an ON state. At the usual bulk NMOS, this voltage is controlled by introduction of the impurities into a silicon substrate. Threshold voltage value can be affected by many factors such as polysilicon type, gate oxide thickness, concentration under the gate and the source and drain (active area). Each factor contribute to different value to threshold voltage, however the source and drain gives a major effect to the threshold voltage value [1]. The result from each parameter in source and drain implant