FACULTY OF ELECTRICAL ENGINEERING

UNIVERSITI TEKNOLOGI MARA

A report submitted to the Faculty of Electrical Engineering, Universiti Teknologi MARA in partial fulfillment of the requirement for the Bachelor of Electrical Engineering (Hons.)

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ACKNOWLEDGEMENTS

In the name of Allah, Most Gracious, Most Merciful. Praised to Prophet Muhammad S.A.W his companions and those who are on the path as what he preached upon. All good aspirations, devotions and prayers are due to ALLAH whose blessing and guidance have helped me throughout the entire project.

I would like to thank Prof. Madya Rosnani Yahya, who has been an inspiration to me in so many ways. As my lecturer and project supervisor she guided me in countless ways. She continually guiding me and encouraging me through some tough situations as well as the support to conduct and finish it. I would also like to thank Dr. Azilah Saparon for his help and guidance using Mentor Graphics software in the past few months.

To my beloved family, especially my parents Ahmad Foat Ibrahim and
who are dearest person in my life and greatest source of inspiration, thank you for the endless love and encouragement they have given and for being so understanding.

And finally but not least, I would like to send a warm thank you to Mohd Razif Kusnin for the valuable help and motivation given in completing this project. As a student, I know it was not easy to give your time, support and lives.

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October 2007

ABSTRACT

This project presents the design, layout, simulation and comparison results of the Folded Cascode Amplifier with a different process variation. Emphasis has been placed on the comparison of the Folded Cascode performance. The Folded Cascode Amplifier structure were designed and laid out in TSMC 0.25μm CMOS technology. While the literature emphasizes is to design the Folded Cascode to meet the best performance. Simulated performance require that the Folded Cascode can obtain equivalent DC gain of 76dB, phase margin 48 degree, Gain Bandwidth 188MHz. power consumption 2.35mW under a 2.5V. The results show that the Folded Cascode has met the specification. Experimental testing needs to be carried out for the further evaluation

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CHAPTER 1

INTRODUCTION

1.2 INTRODUCTION

CMOS operational amplifier (op-amp) is often preferred as "building blocks" in circuits for analog applications due to dense, low voltage and low power features of CMOS process. But the MOS transistors are "noisy", moreover, as MOS device sizes and signal levels are aggressively scaled down, the low frequency noise (LFN) properties become increasingly important, especially in professional audio systems, and precise medical diagnostic systems [13].

For this, the analog designers are facing a formidable challenge, how to design low noise operational amplifier, while taking advantage of the unique features of the CMOS technology. In CMOS operational amplifier, low frequency noise is usually dominated by flicker noise. In [13-16], low noise CMOS operational amplifier design has been studied. Low noise operational amplifier design practice often adopts large size p-channel input transistors with high trans-conductance whenever possible [14]. But input capacitance will distinctly increase with the area of input transistor increasing and result in speed penalty.

Moreover, this defeats the major objective of scaling. An alternative to large geometry MOS transistors is using lateral p-n-p bipolar transistors as the input transistors [3-5]. But this process is complicate, and large bipolar base currents and parasitic vertical collector currents also limit their application in CMOS analog circuit design.

In [15], MOSFET transistors operating in the sub-threshold region have been used as input devices to create low noise operational amplifier and have exhibited similar characteristics to a bipolar transistor without requiring the relatively large base current of bipolar transistor to operate, however, many